PSLP: Padded SLP Automatic Vectorization

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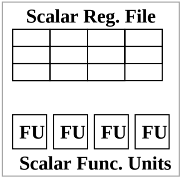
University of Cambridge[†]
University of Edinburgh[‡]

EuroLLVM APR 2015

Why SIMD Vectorization?

- Scalable parallelism



a. ILP

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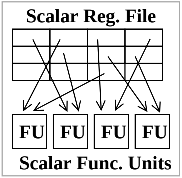

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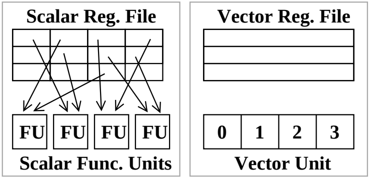

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b. Vector Parallelism

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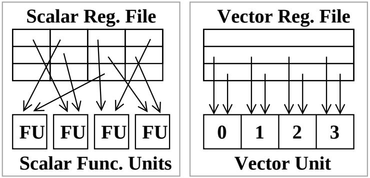

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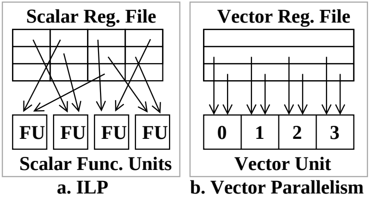

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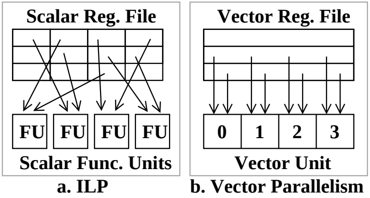
- Energy efficiency



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- High Performance
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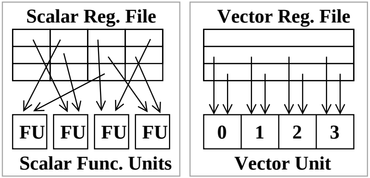
- Supported since mid 90's
- Frequent updates of vector ISAs



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AMD K6-2 PROCESSOR 3DNOW!

ARM NEON™

AVX2

MMX™ intel inside pentium PROCESSOR

altivec™ technology

SSE4

Why SIMD Vectorization?

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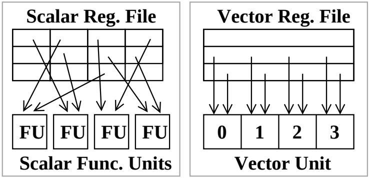
- Supported since mid 90's
- Frequent updates of vector ISAs
- Vector generation not done in hardware
- Low-level programming or capable compiler



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- In theory it should be a superset of loop-vectorizer
  - Unroll loop and vectorize with SLP
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- In practice it is missing features present in the Loop vectorizer (Interleaved Loads, Predication)

SLP Vectorization Algorithm

- Input is scalar IR

Scalar Code

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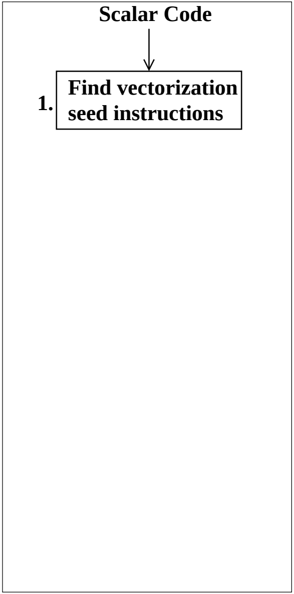
  1. Consecutive Stores
  2. Reductions



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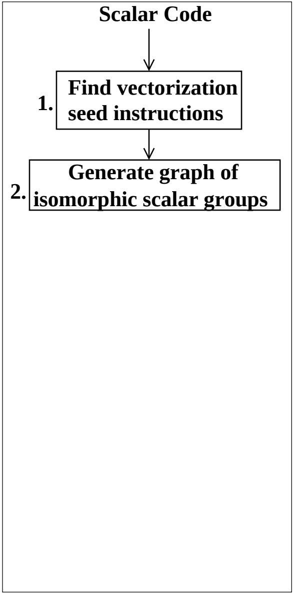

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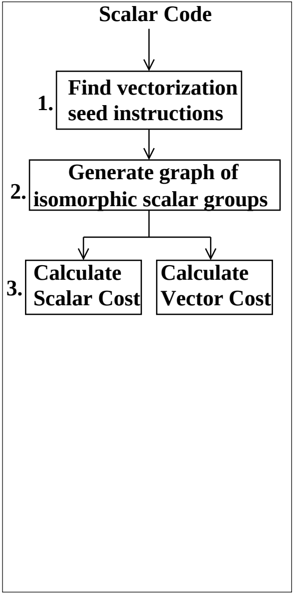

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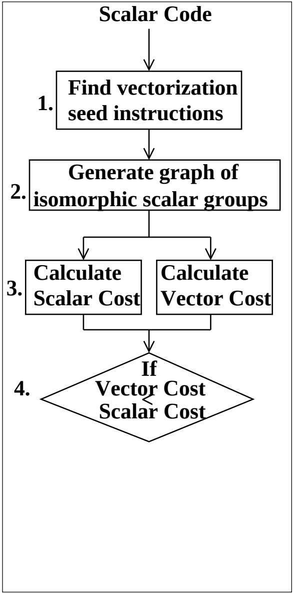

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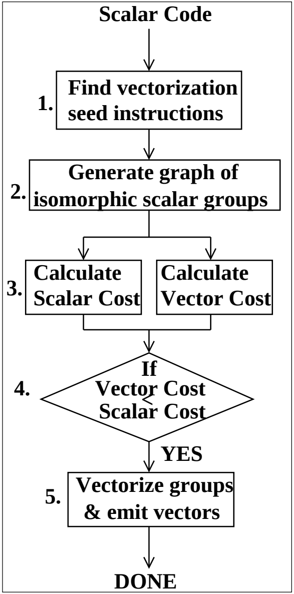

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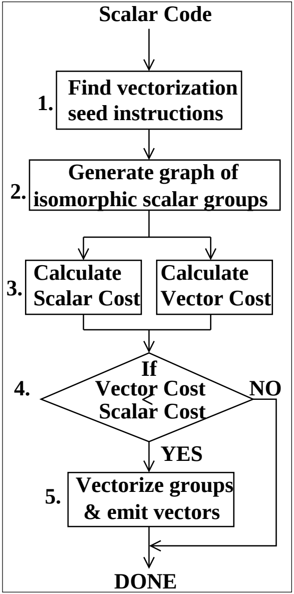

When SLP Fails

1. Data Dependencies

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2. Too many gather/scatter instructions. Costs outweigh benefits.

Original	Vectorized
ADD1	Insert1
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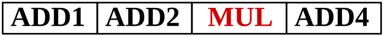
3. Non-isomorphism



SLP Fails due to non-isomorphism

```
      ...
B[i]   = A[i]   * 7.0 + 1.0;
B[i+1]= A[i+1]        + 5.0;
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a. Input C code

(X) **Instruction Node or Constant**	→ **Data Flow Edge**

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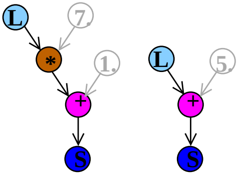

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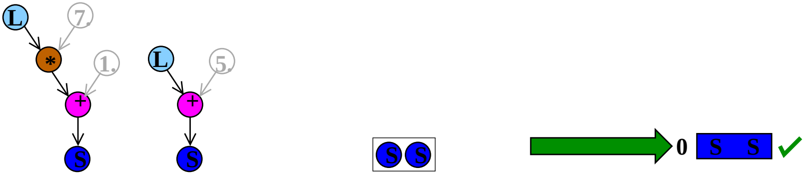

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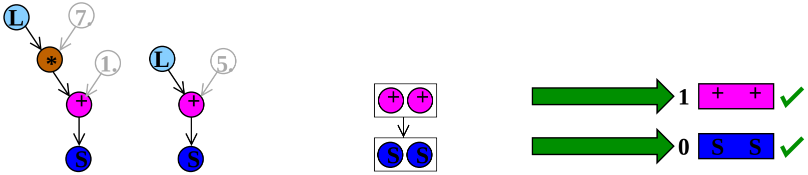

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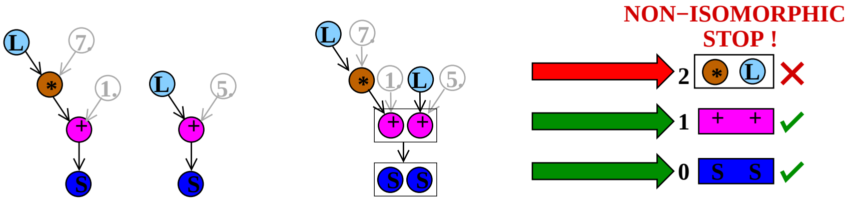

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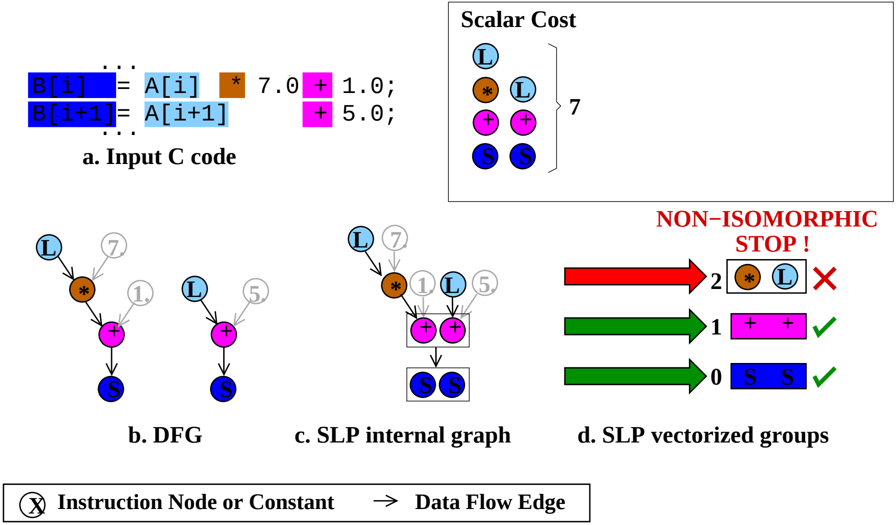

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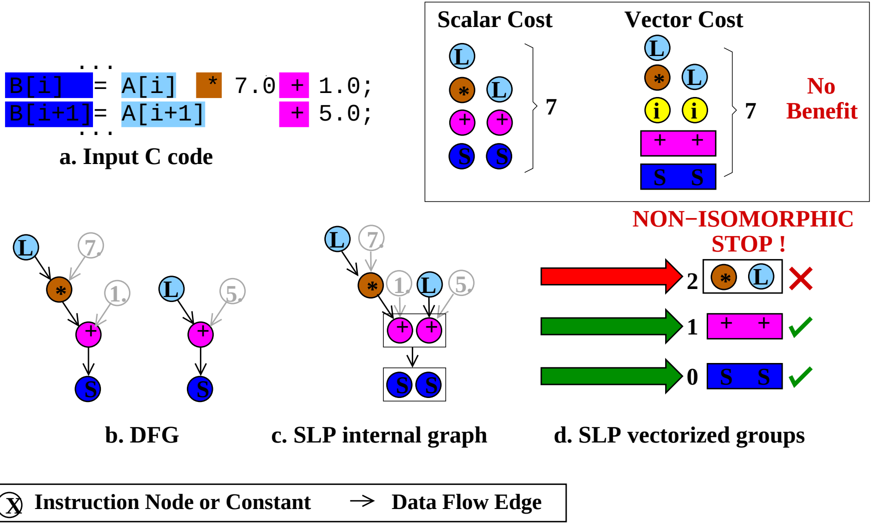
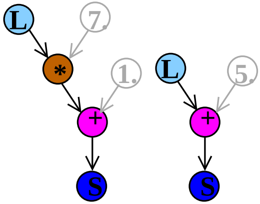


PSLP fixes Non-Isomorphism



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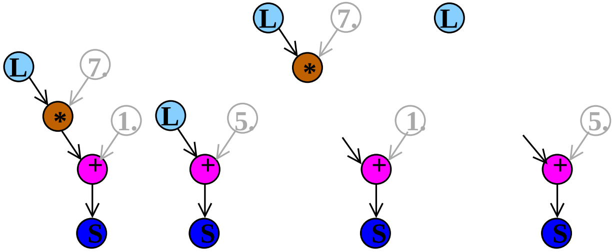

a. PSLP graphs

b. PSLP padded graphs

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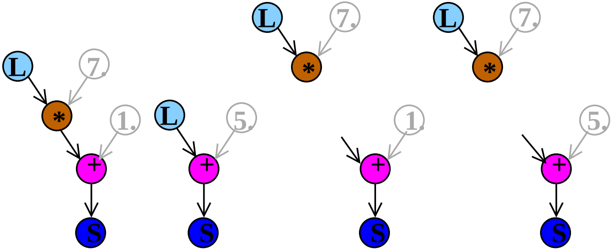

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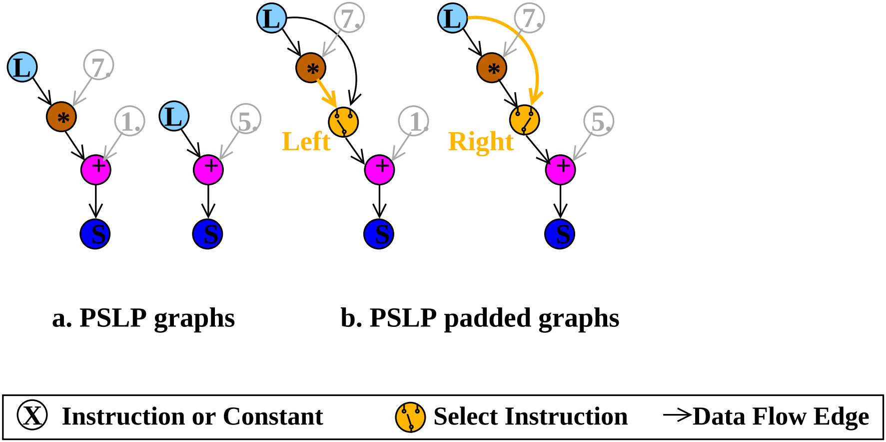

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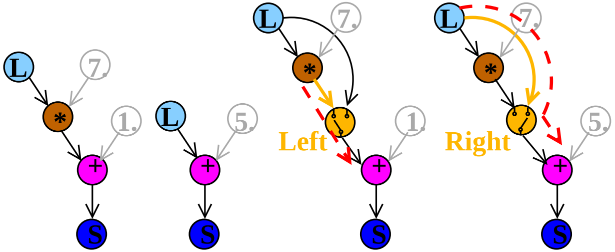

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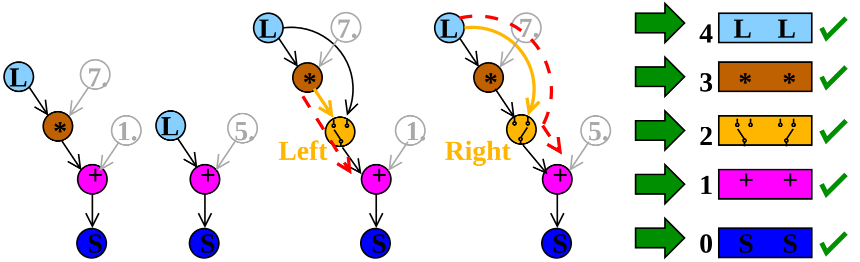

a. PSLP graphs b. PSLP padded graphs c. PSLP groups

X Instruction or Constant Select Instruction → Data Flow Edge

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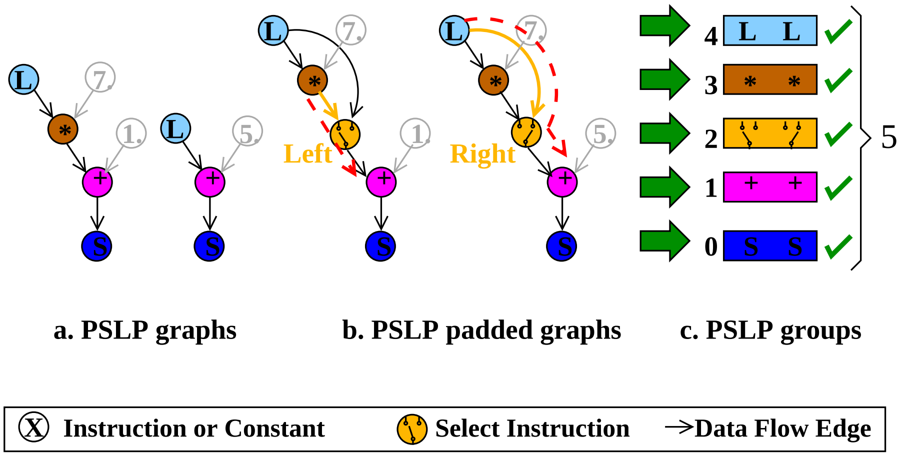

PSLP Algorithm

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1. **Find vectorization seed instructions**

PSLP Algorithm

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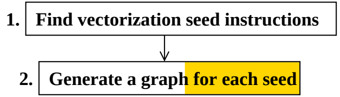
- Generate multiple graphs (unlike SLP)



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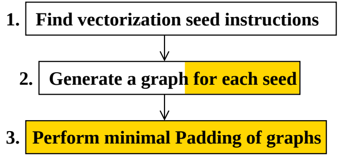

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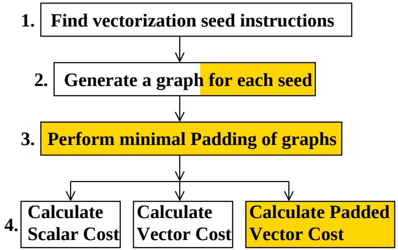

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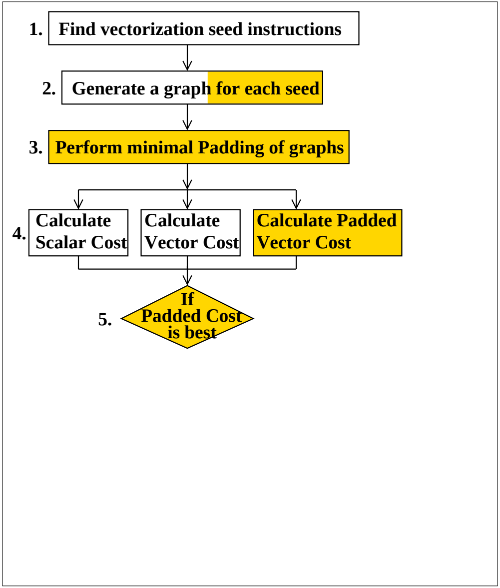

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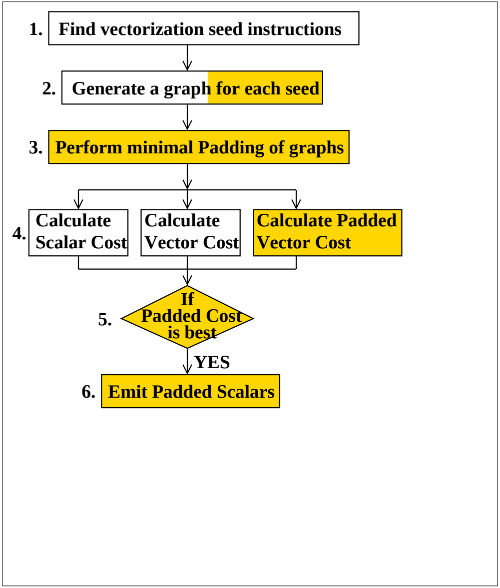
- Emit redundant code to create isomorphism



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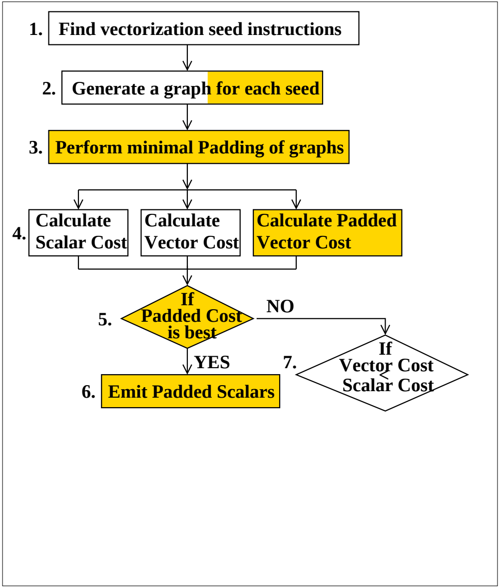

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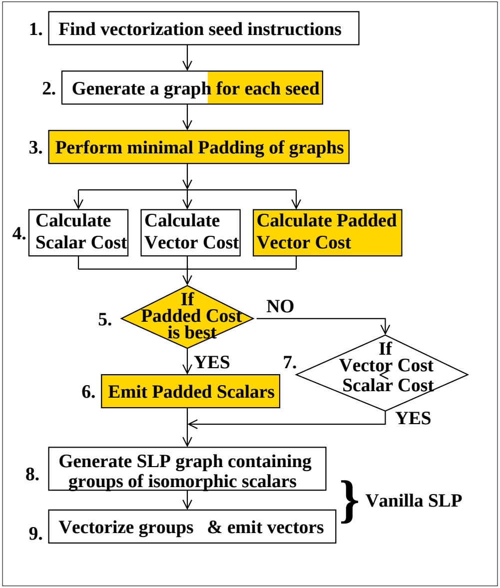

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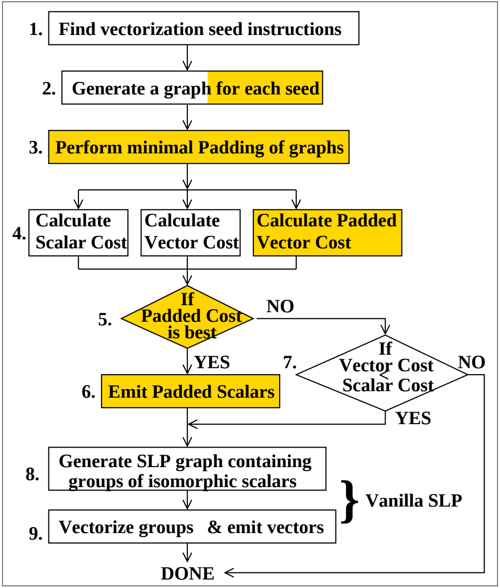

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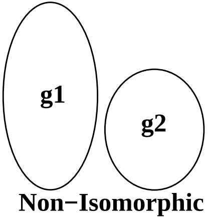

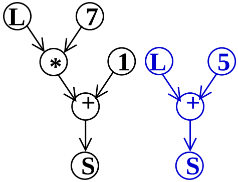

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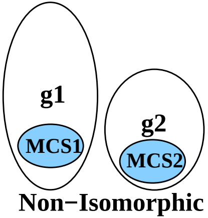

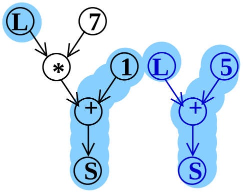

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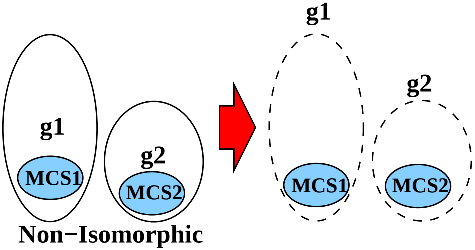

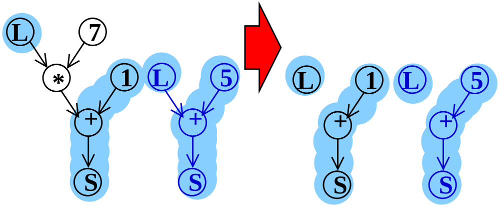

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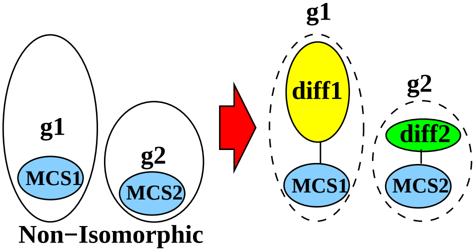

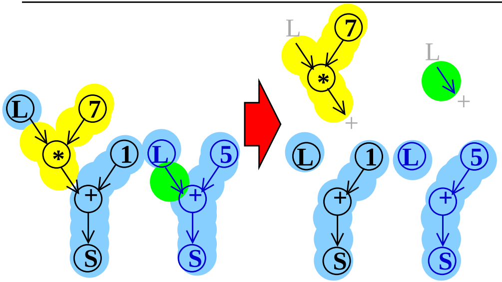

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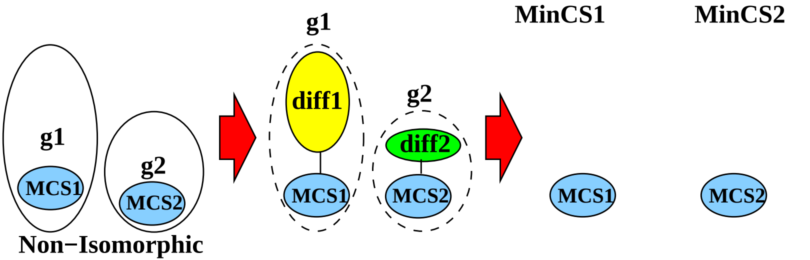

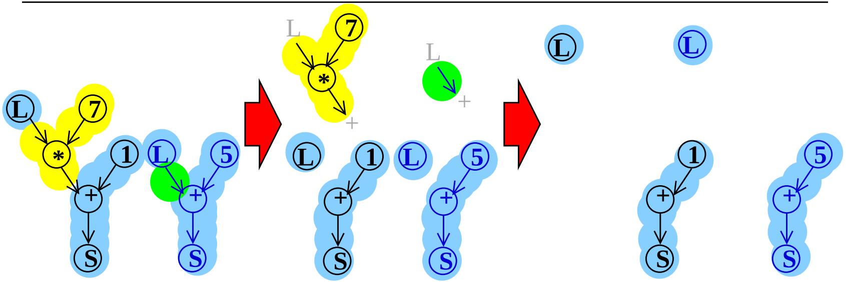

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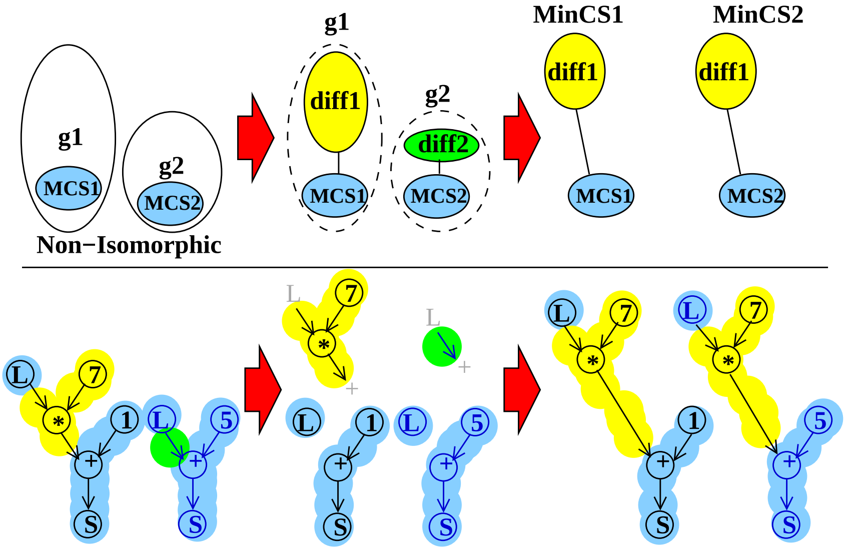

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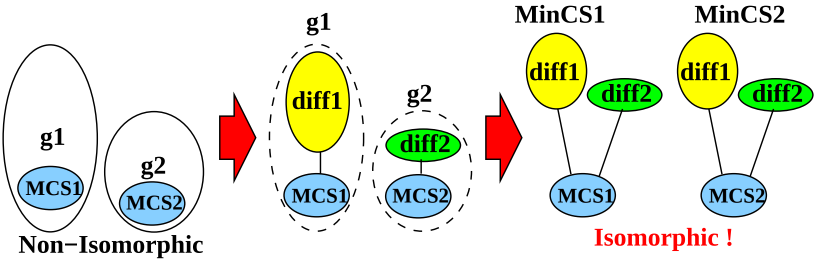

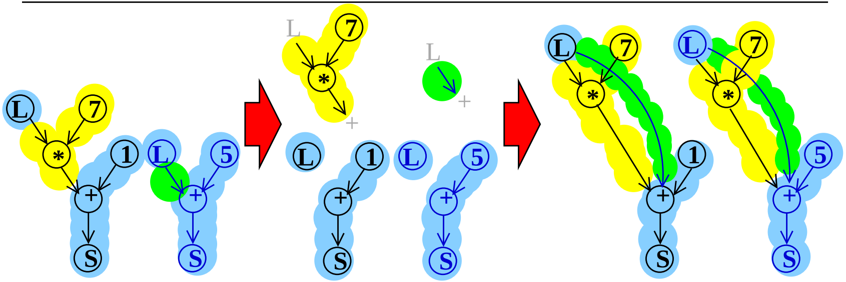

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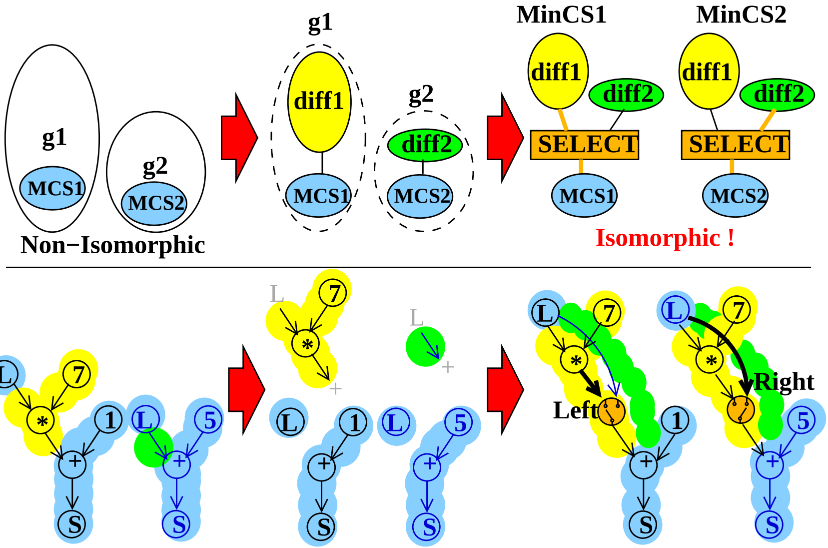
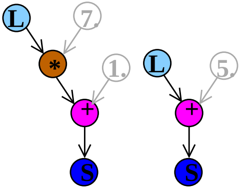


We can do better: Remove redundant Selects



EXAMPLE: Instruction acting as Select

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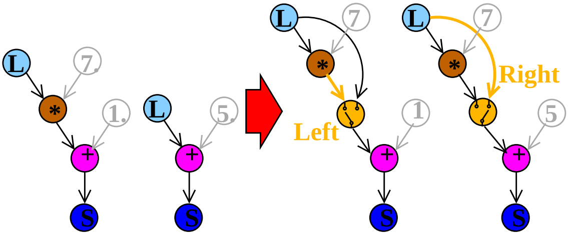

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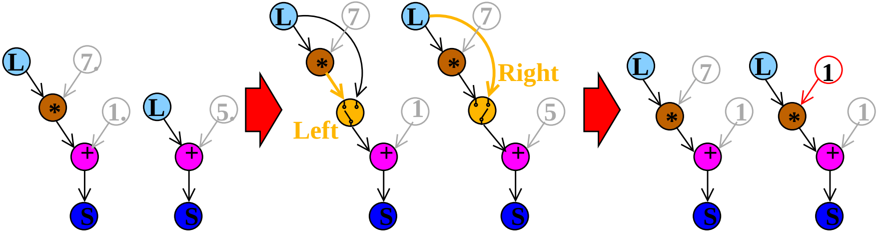

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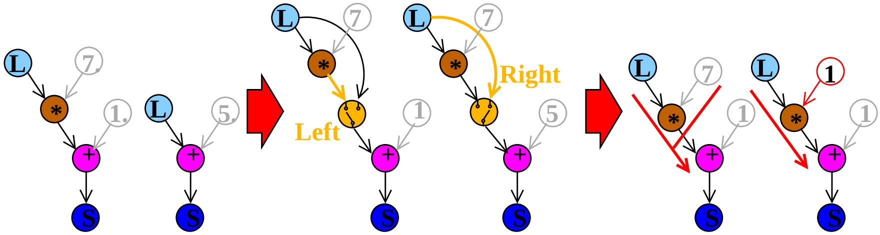

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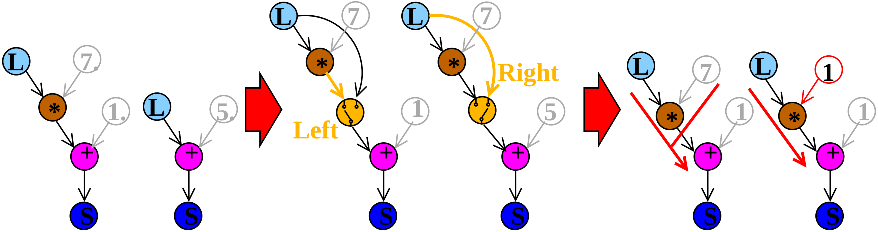

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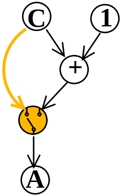

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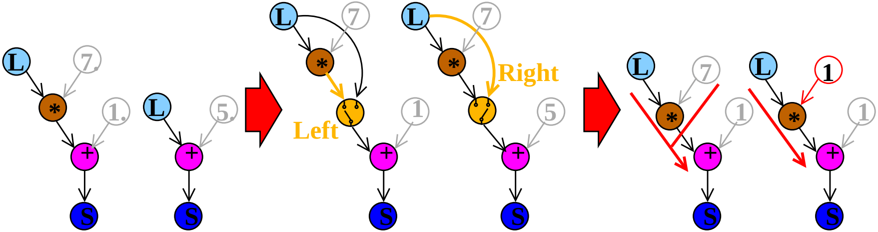

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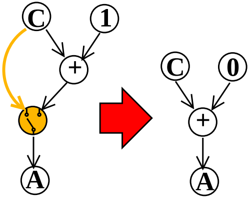

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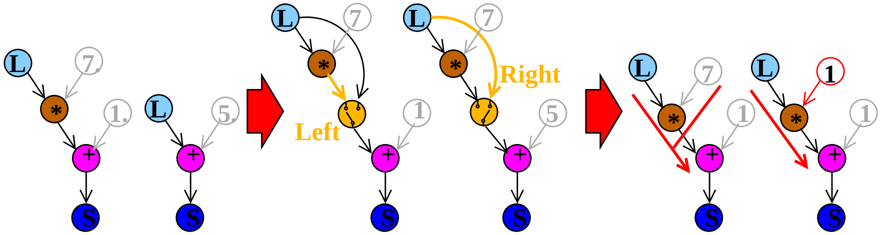

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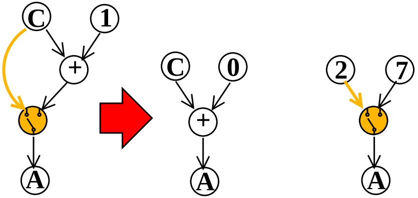

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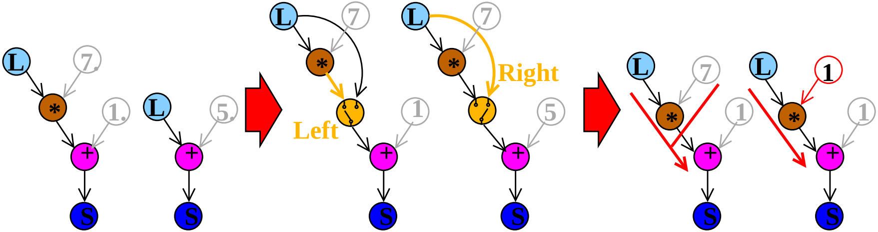

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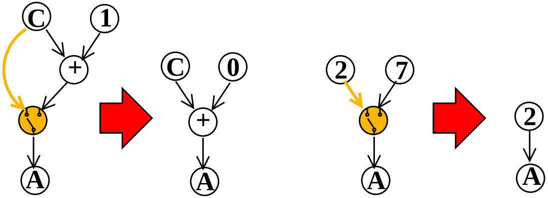

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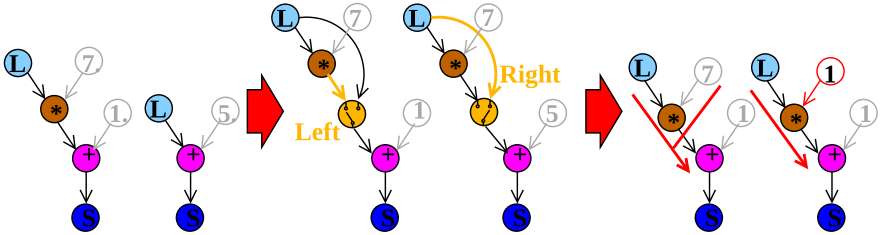

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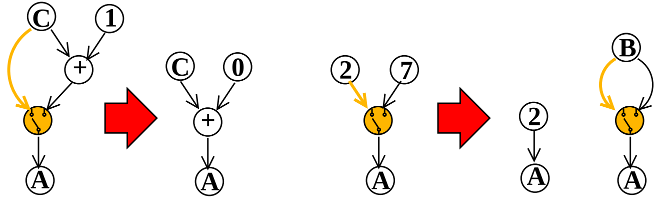

a. Instruction acting as Select b. Select constants c. Select same node

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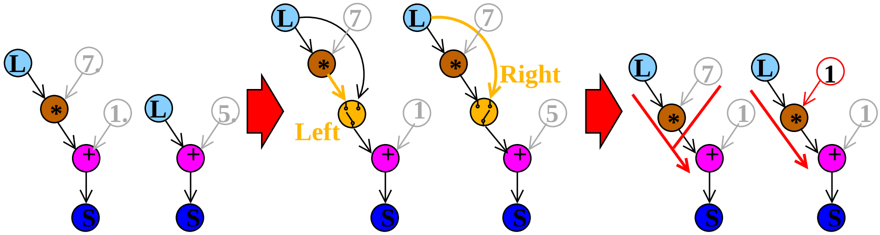

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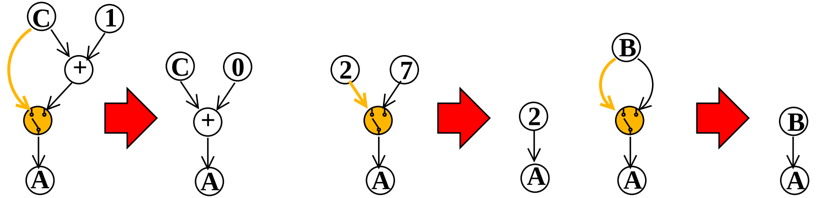

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Opportunities for PSLP in real-life applications

1. Non-isomorphic source code (e.g. computing conjugates in 433.milc)

```
b[0].real =   a[0].real
b[0].imag = - a[0].imag
b[1].real =   a[1].real
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```

Memory
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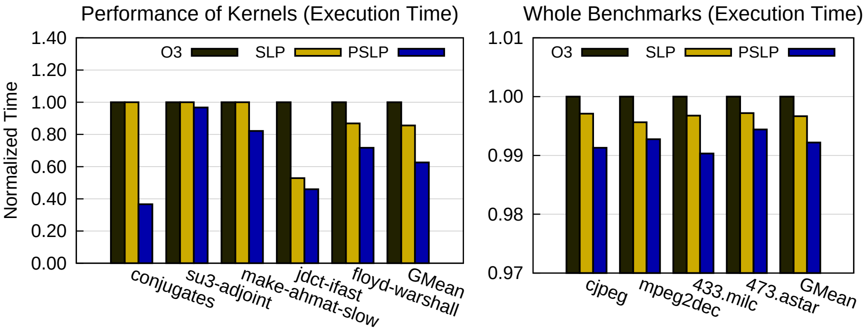
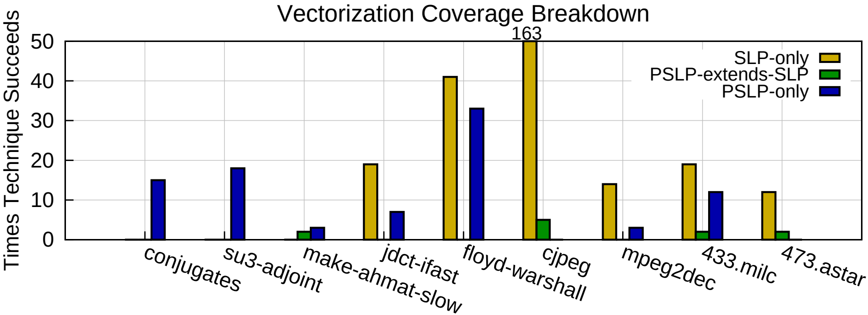
  3. O3 + PSLP enabled (PSLP)

PSLP increases performance



PSLP enables or extends vectorization



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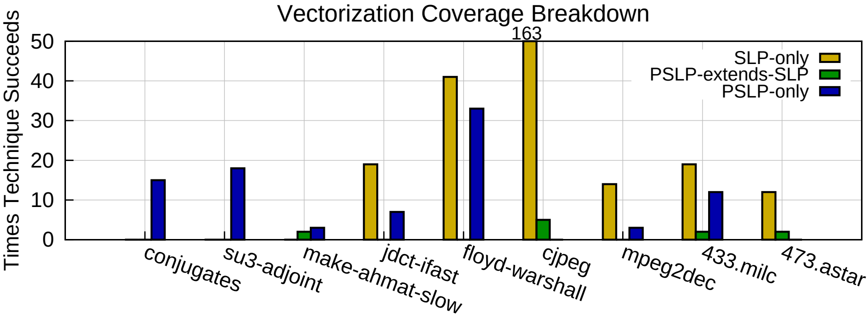

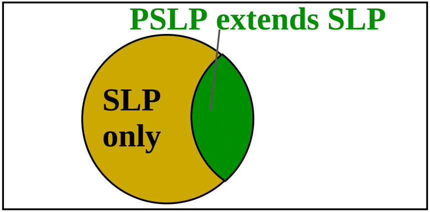

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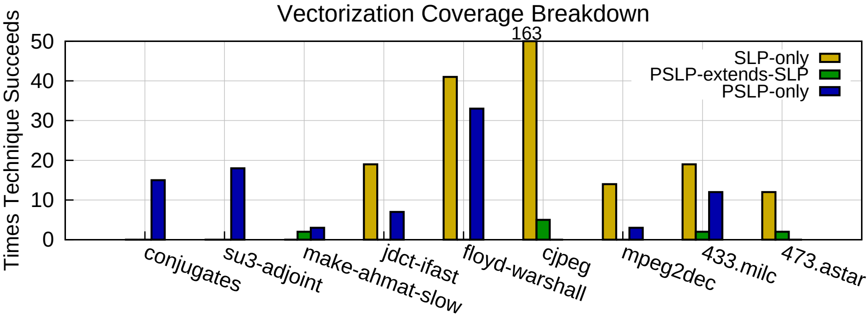

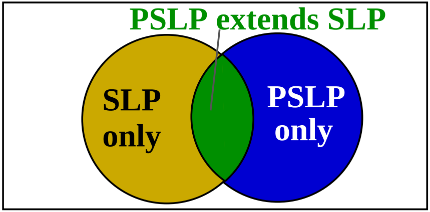

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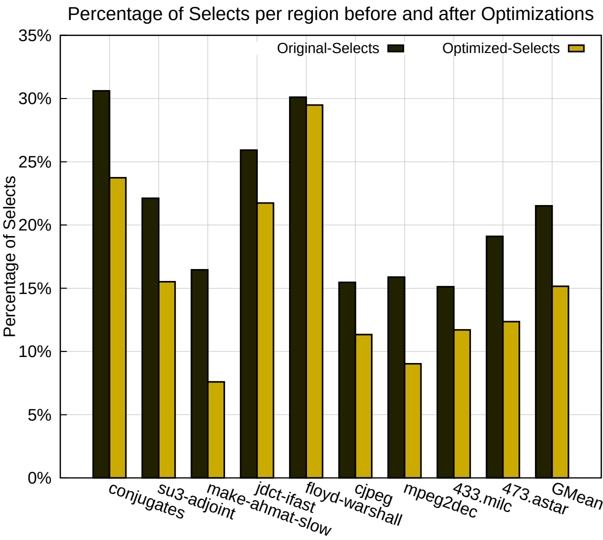
- SLP fails completely. PSLP succeeds.

Optimizing away redundant Selects

- Select-removal optimizations remove about 21% of the Selects



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- PSLP performs better compared to SLP on commodity SIMD-capable hardware