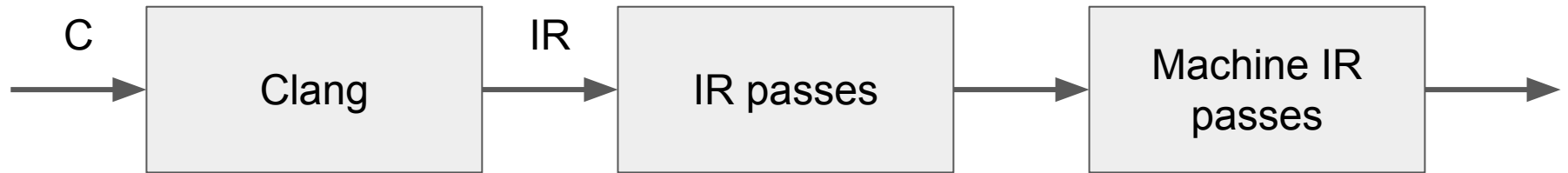
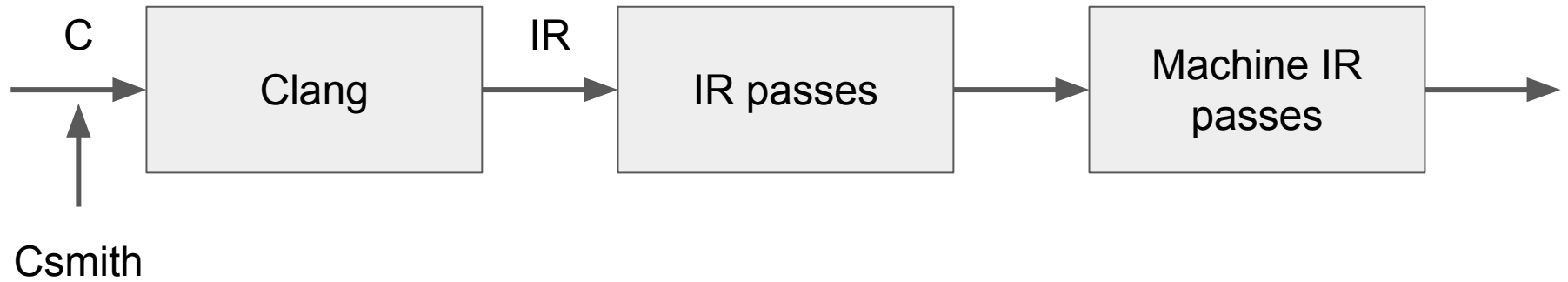


Random Testing of the LLVM Code Generator

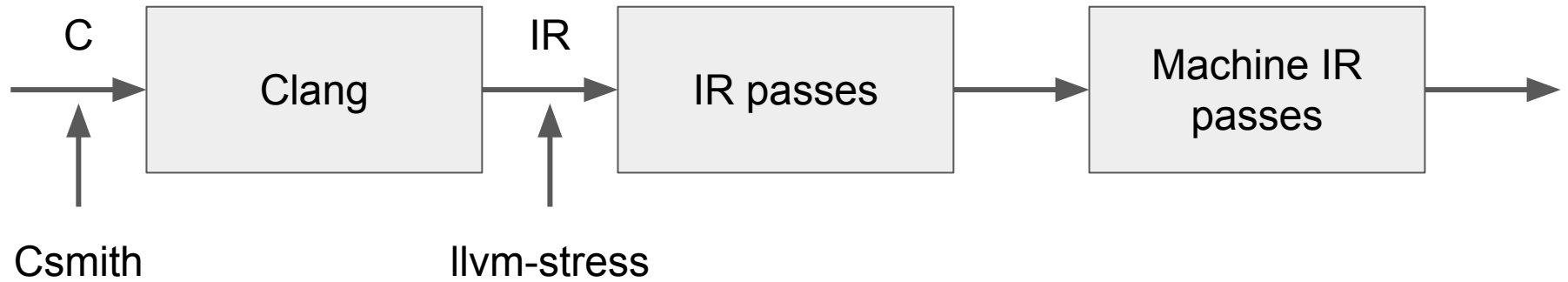
Random testing is useful



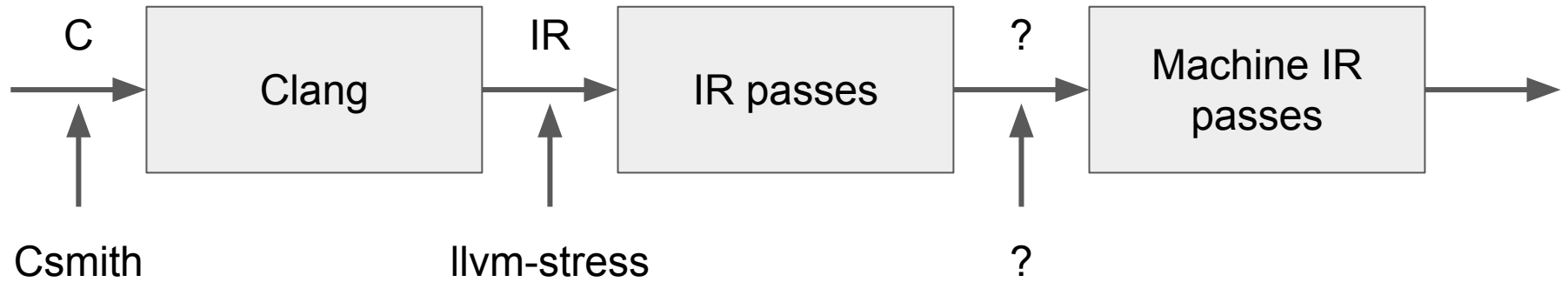
Random testing is useful



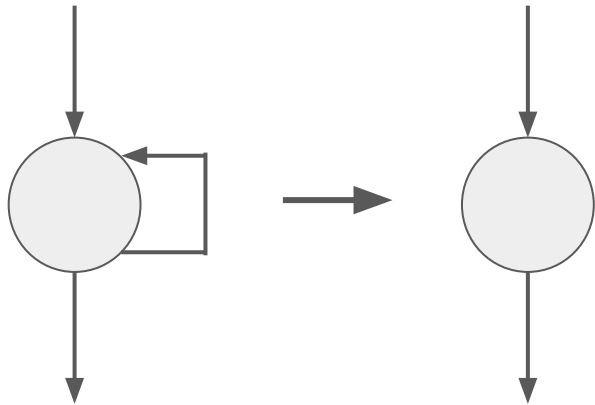
Random testing is useful



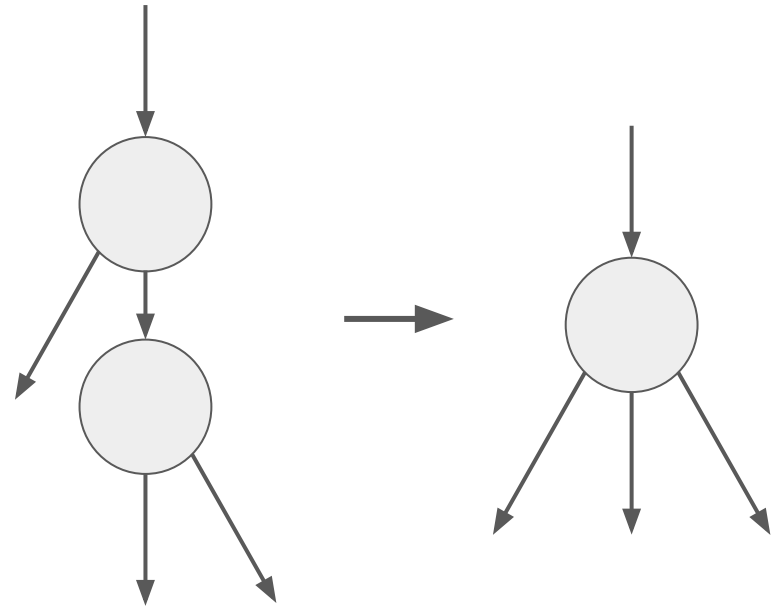
Random testing is useful



Reducibility

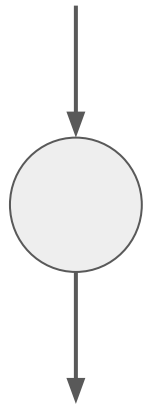
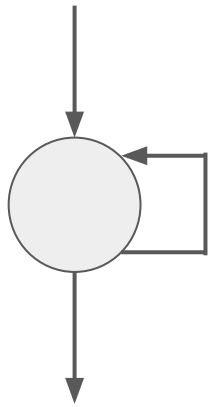


T1

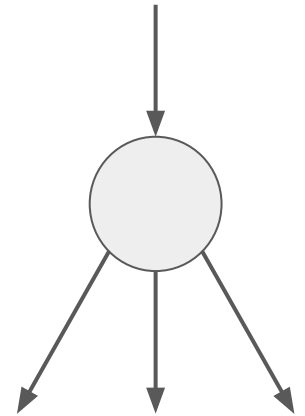
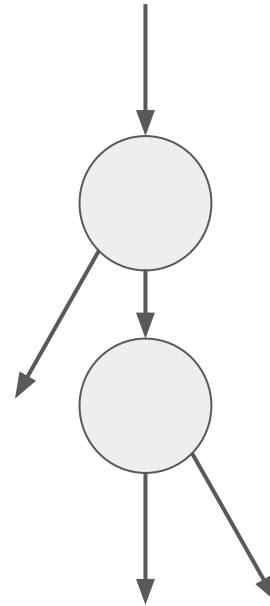


T2

Inverse reducibility transform generation

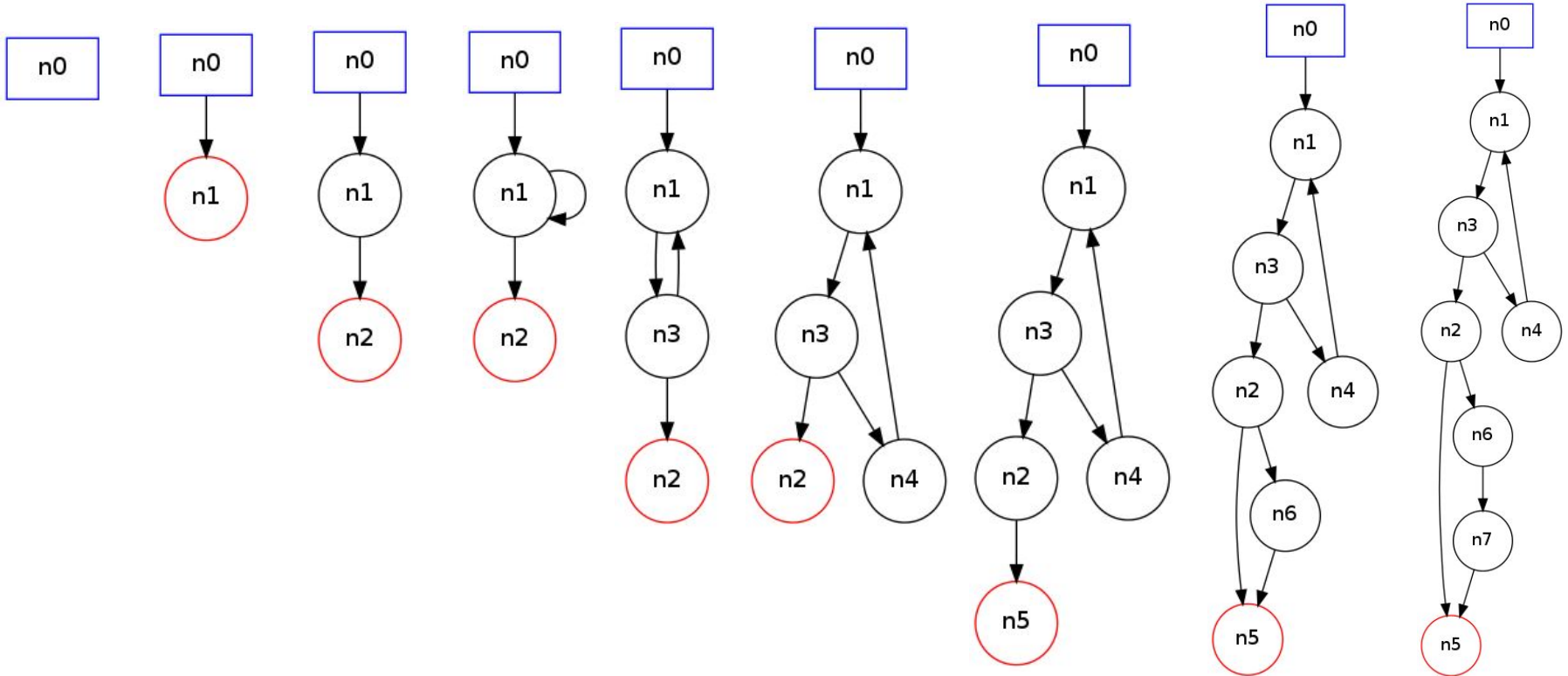


T1

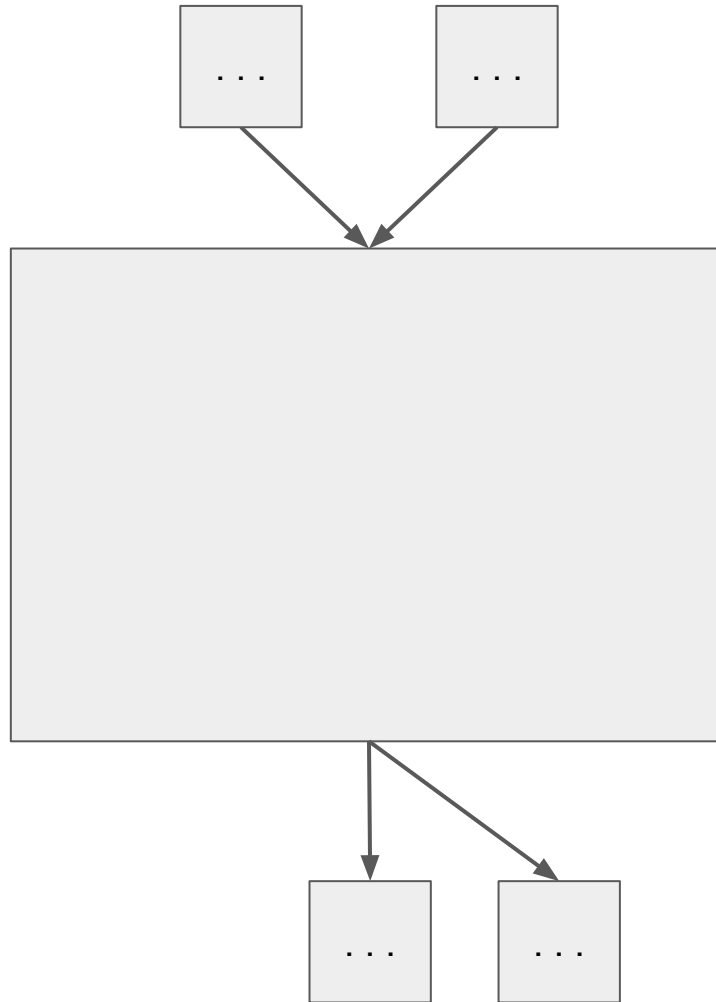


T2

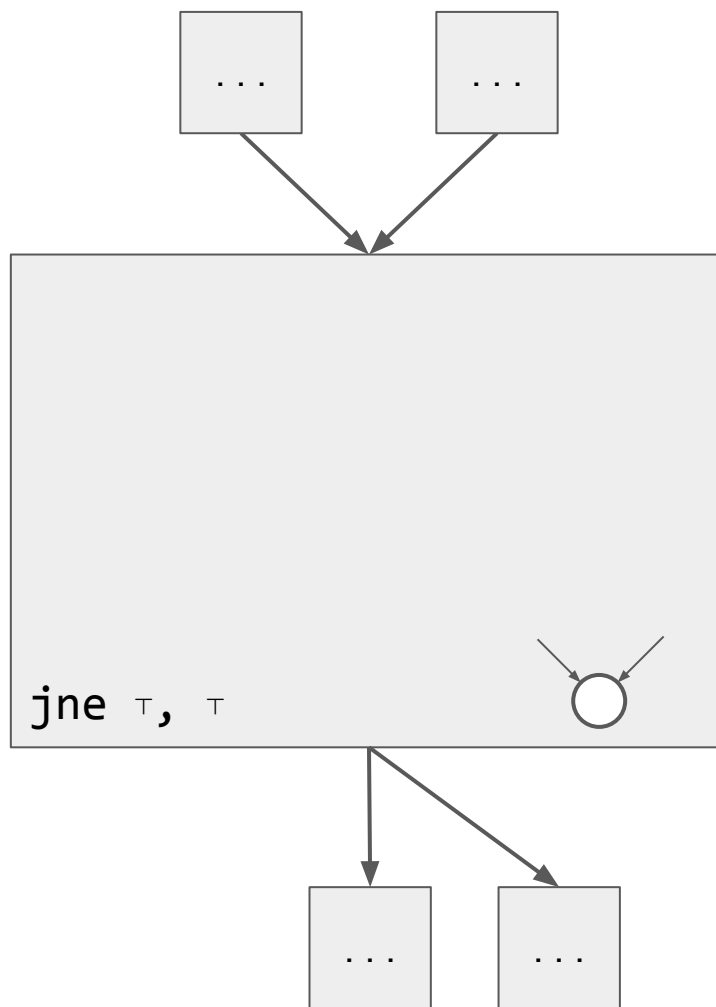
Inverse reducibility transform generation



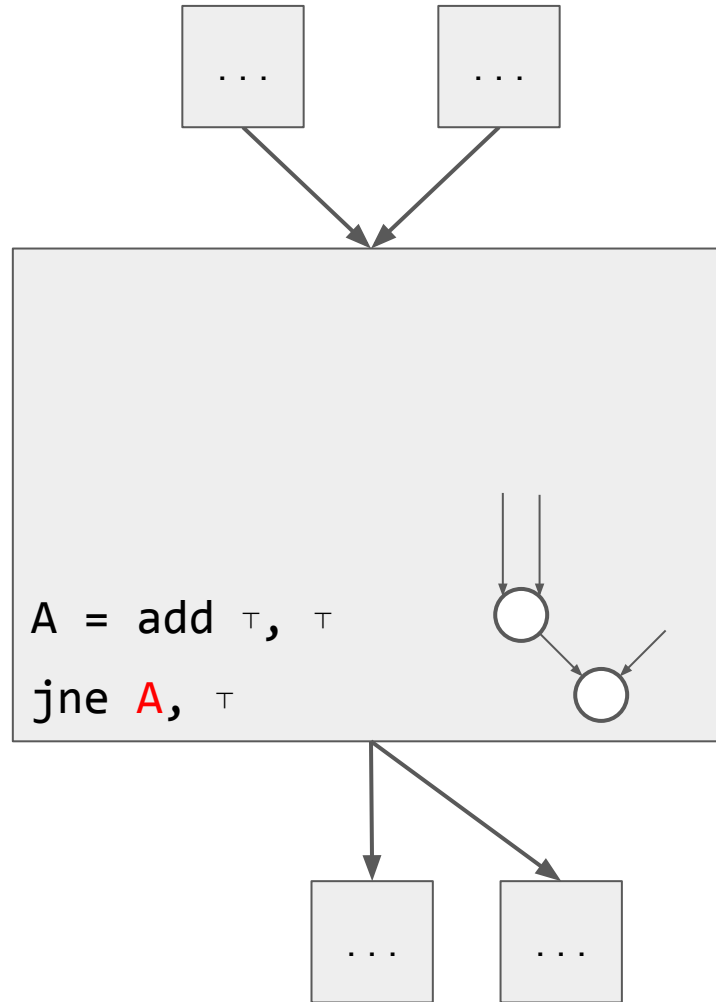
Fixedpoint bottom-up data flow generation



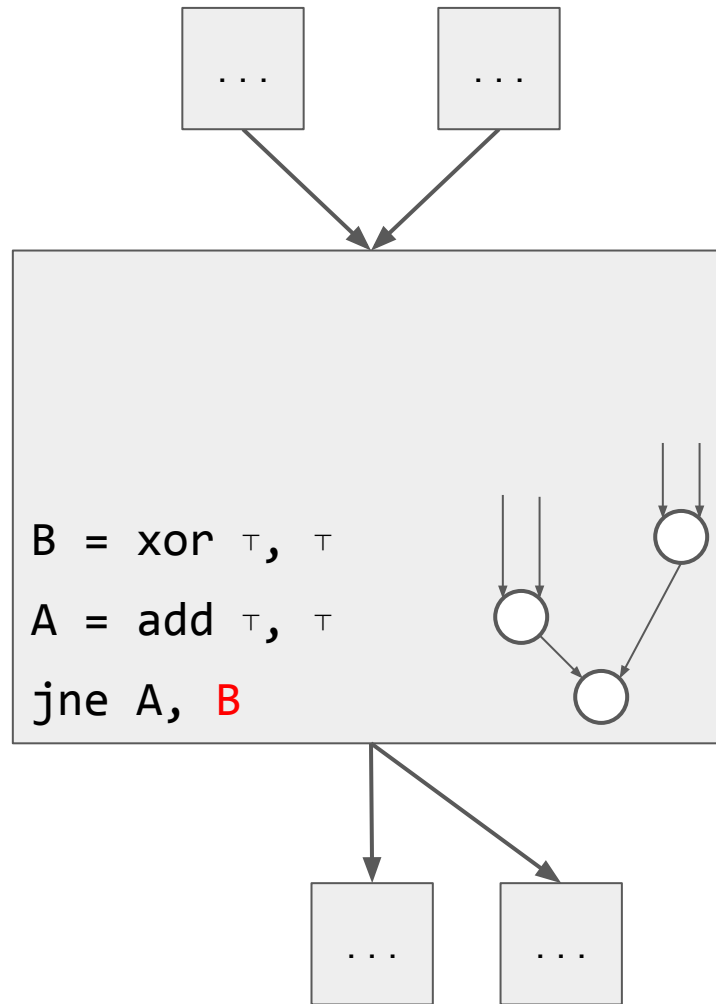
Fixedpoint bottom-up data flow generation



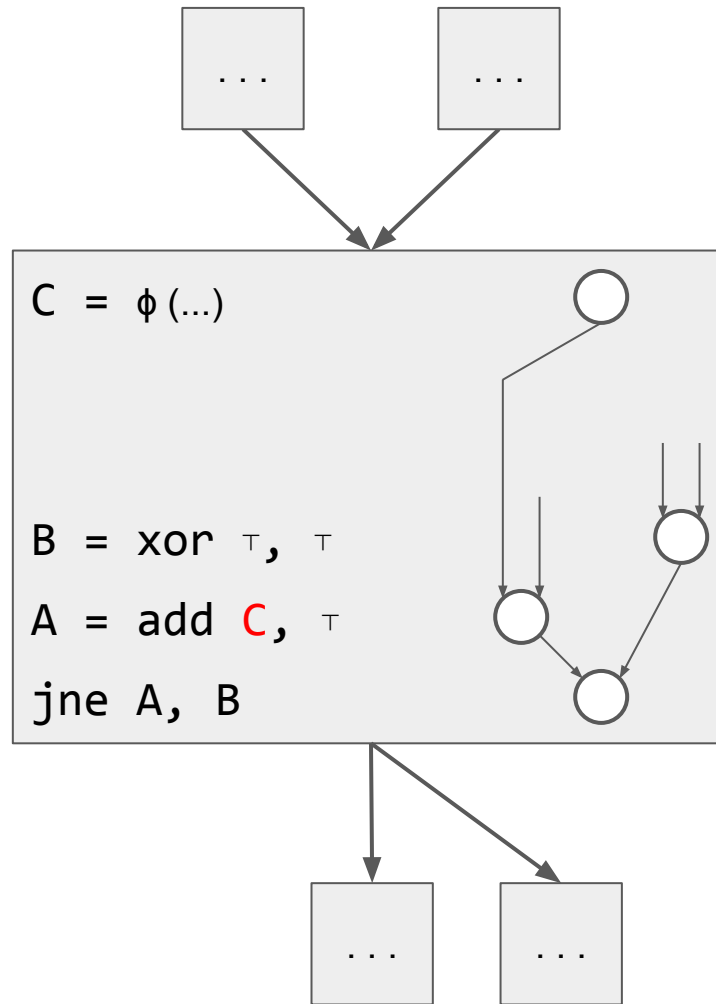
Fixedpoint bottom-up data flow generation



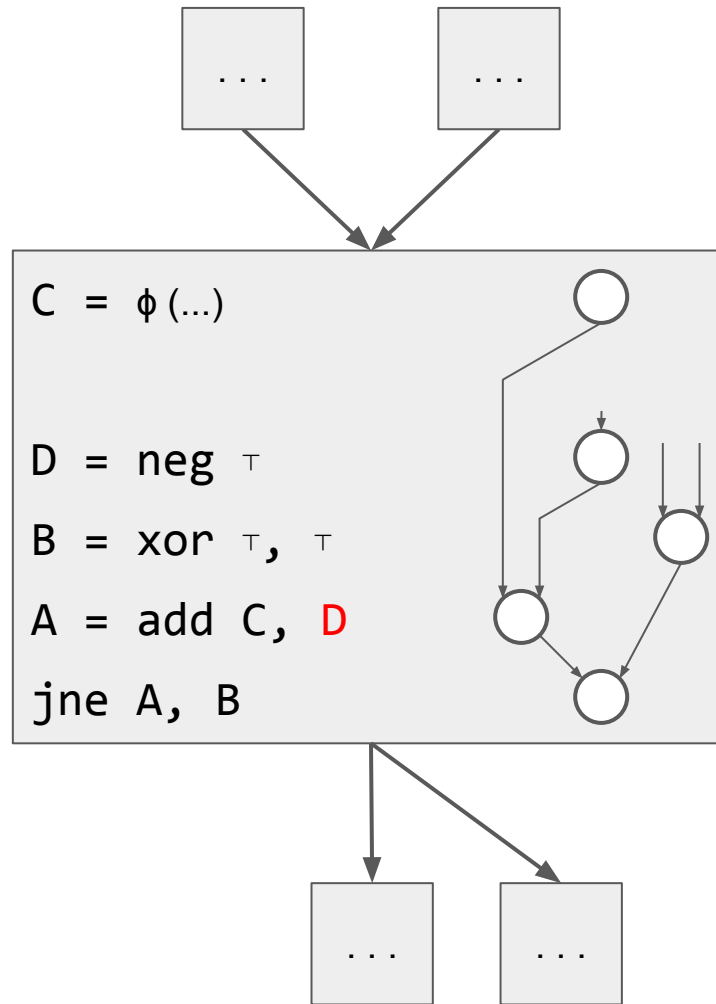
Fixedpoint bottom-up data flow generation



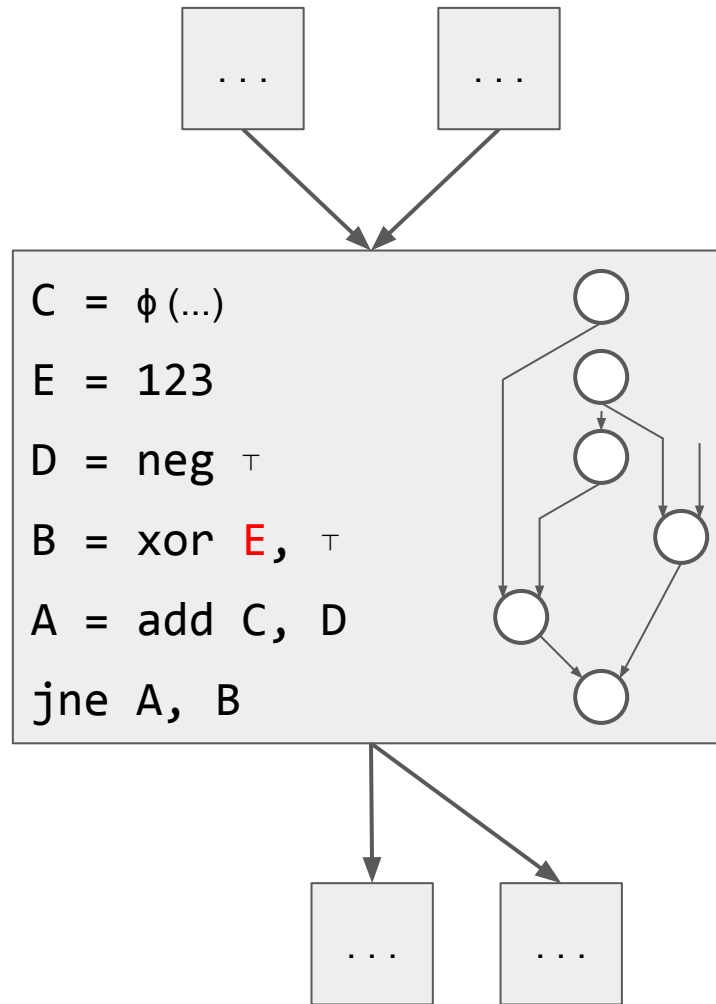
Fixedpoint bottom-up data flow generation



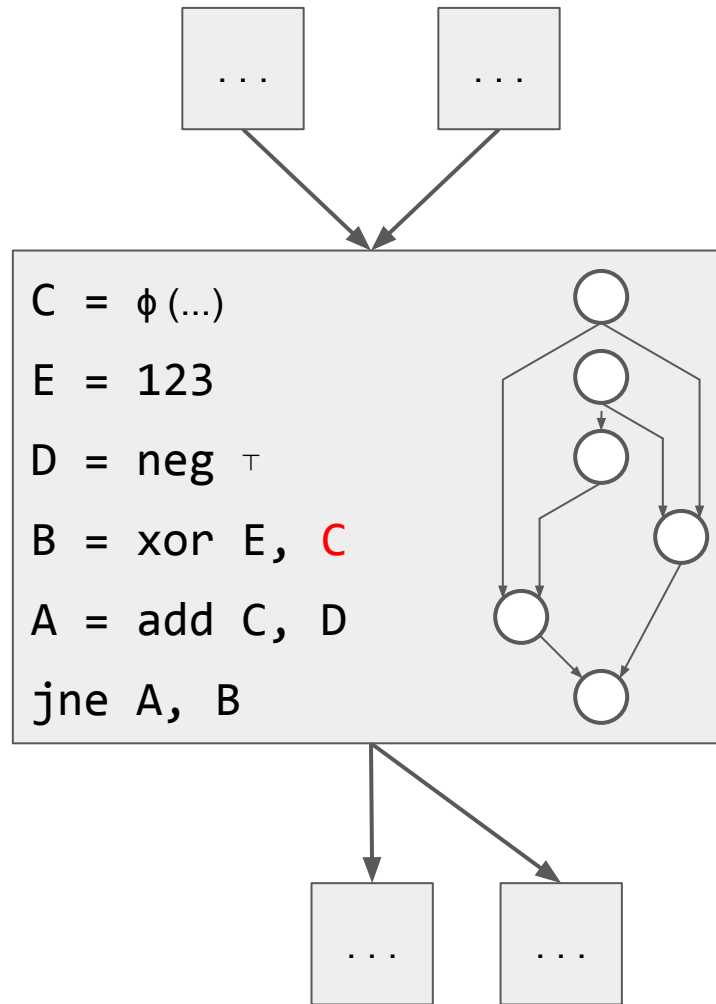
Fixedpoint bottom-up data flow generation



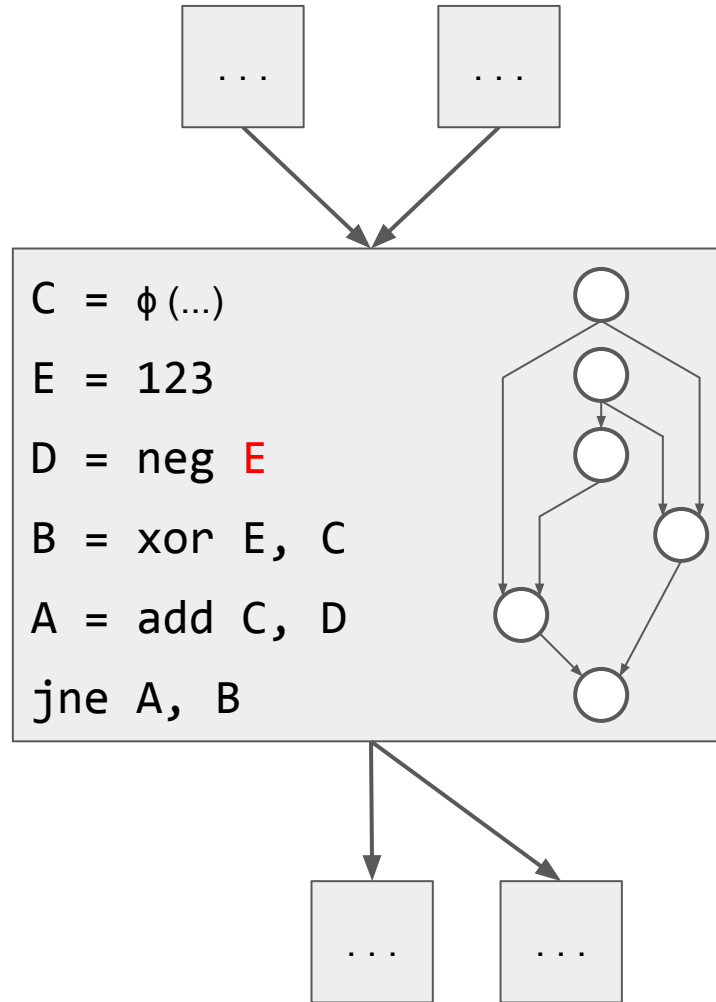
Fixedpoint bottom-up data flow generation



Fixedpoint bottom-up data flow generation



Fixedpoint bottom-up data flow generation



Conclusion

- A textual representation of Machine IR was designed
- A Hexagon implementation of random generation was made
- Testing discovered some assertion failures, but no bugs
- Perhaps the new textual MIR implementation could yield better results
- Or: redesign llvm-stress with these methods in mind