Optimal Register Allocation and Instruction Scheduling for LLVM

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joint work with:

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C. Schulte – KTH, SICS

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Code Generation in LLVM

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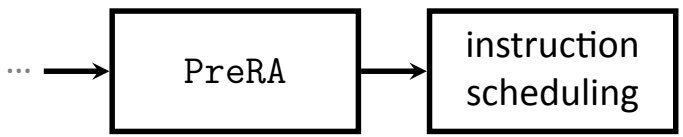

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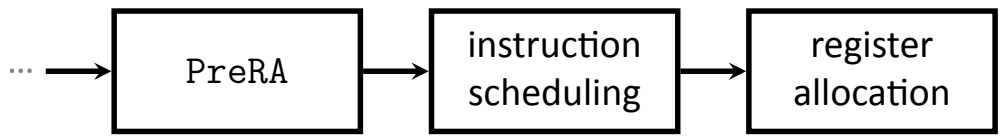

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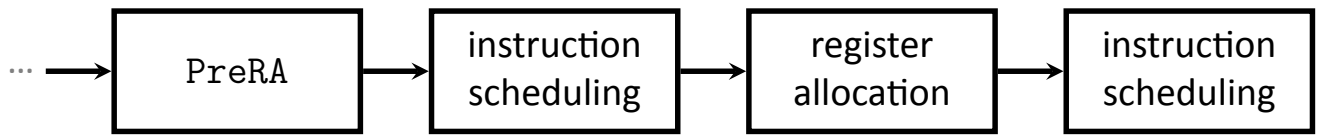

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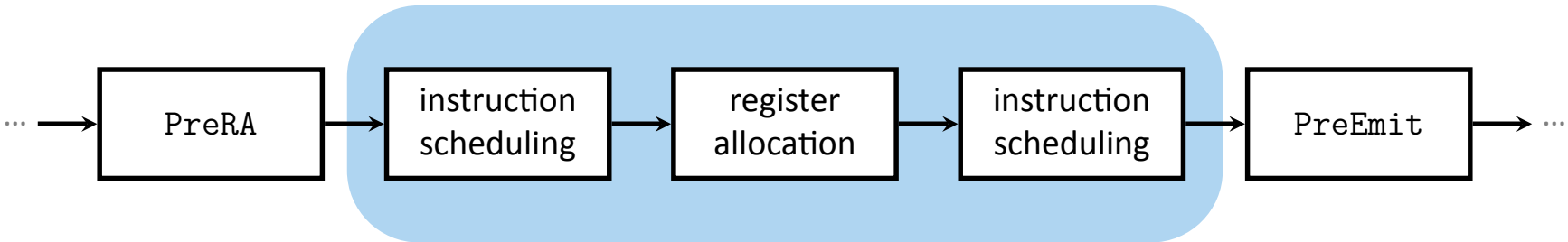

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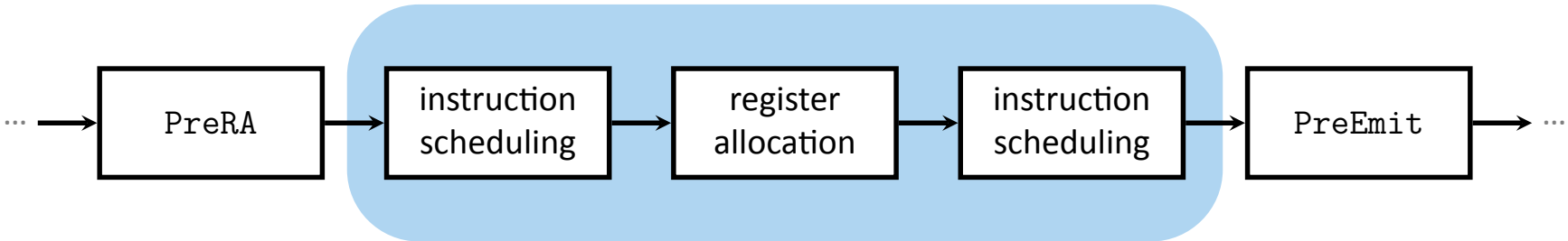

- Stages, heuristics

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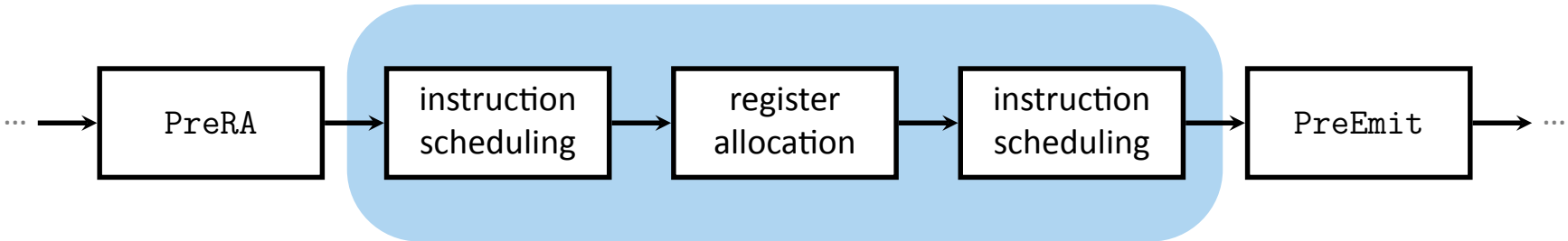

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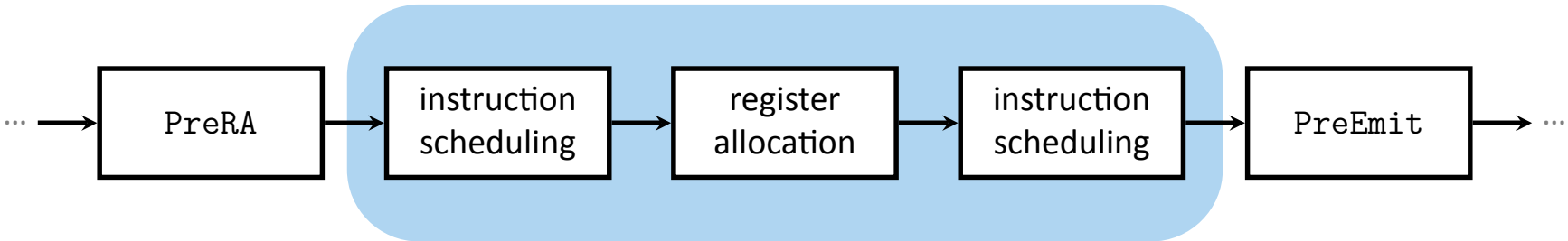

- Stages, heuristics
- Pros: compilation speed
- Cons: suboptimal, complex

Introducing Unison

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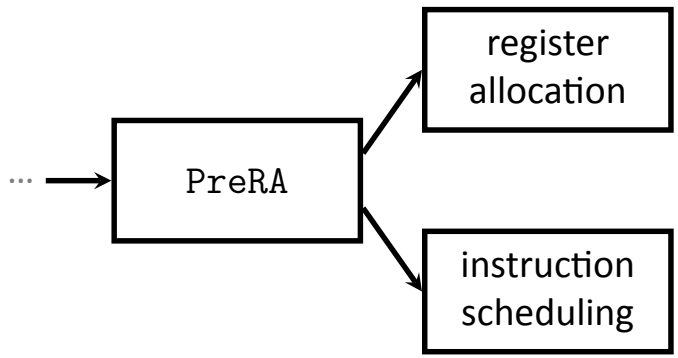

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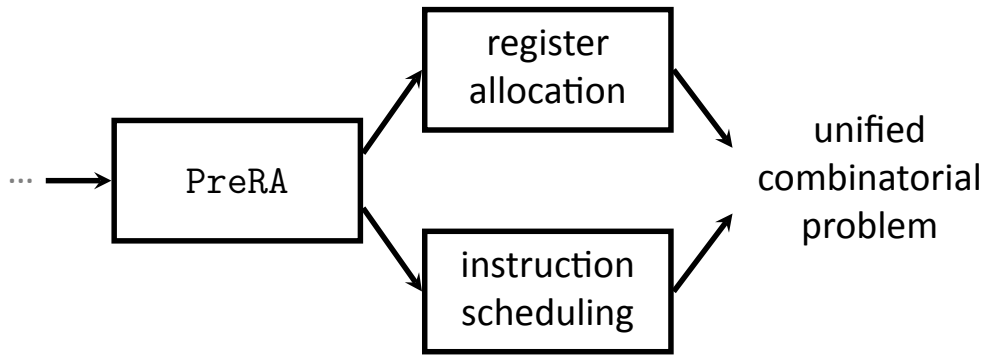

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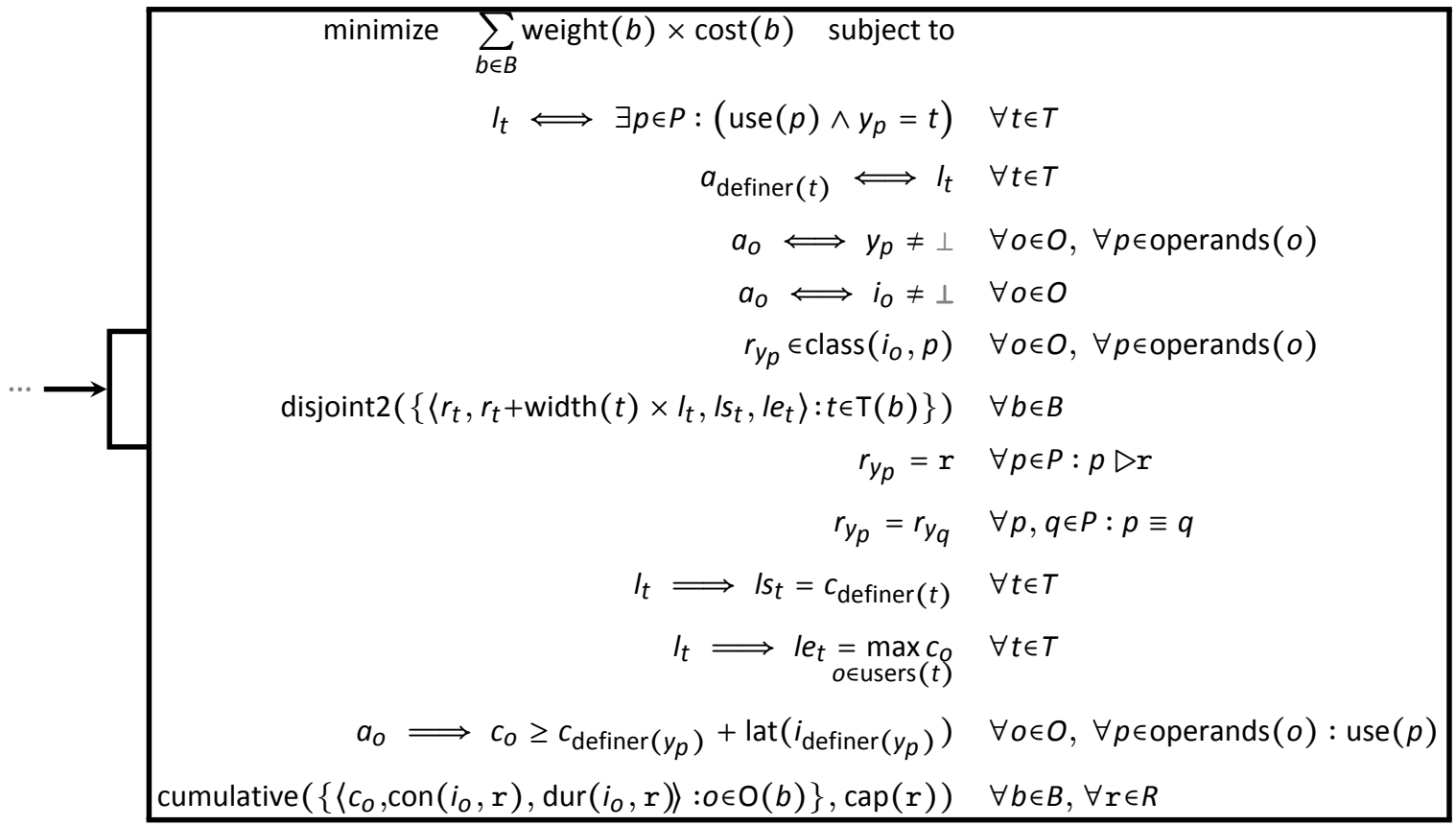

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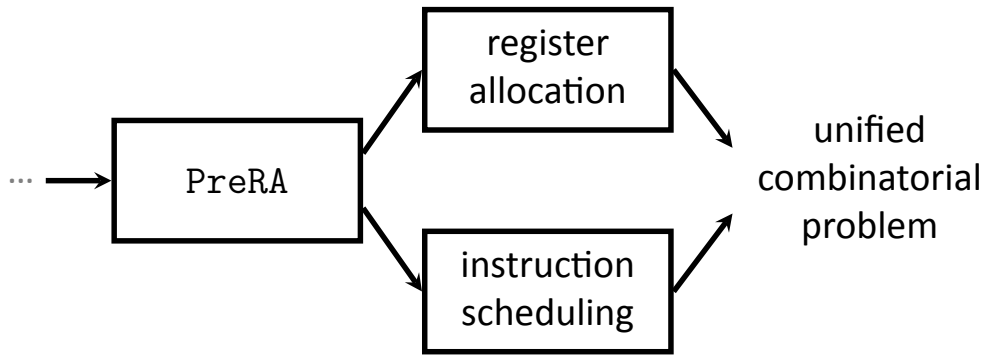

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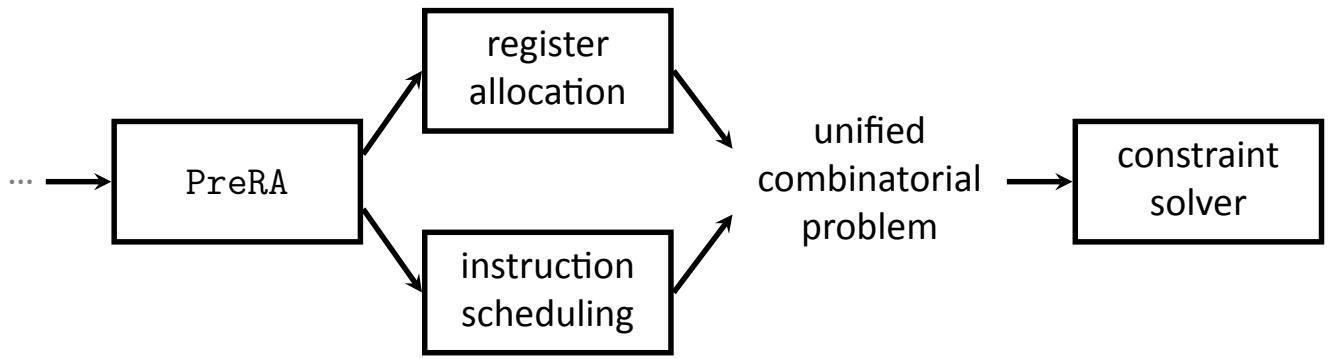

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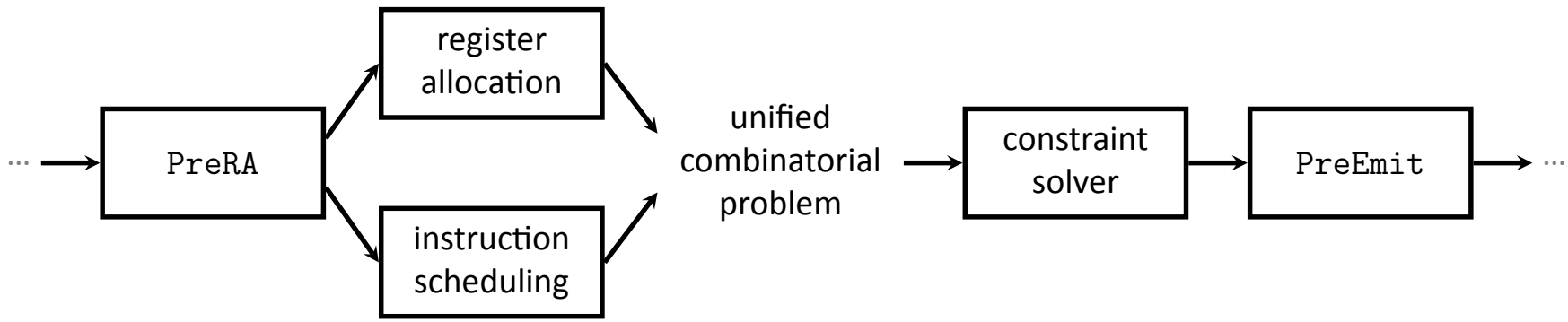

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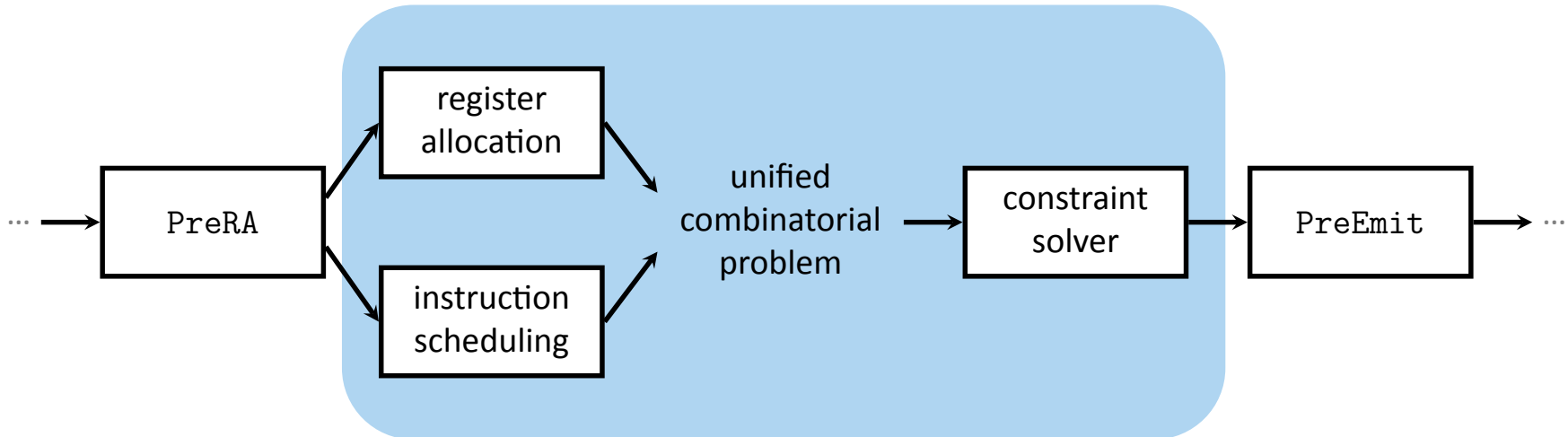

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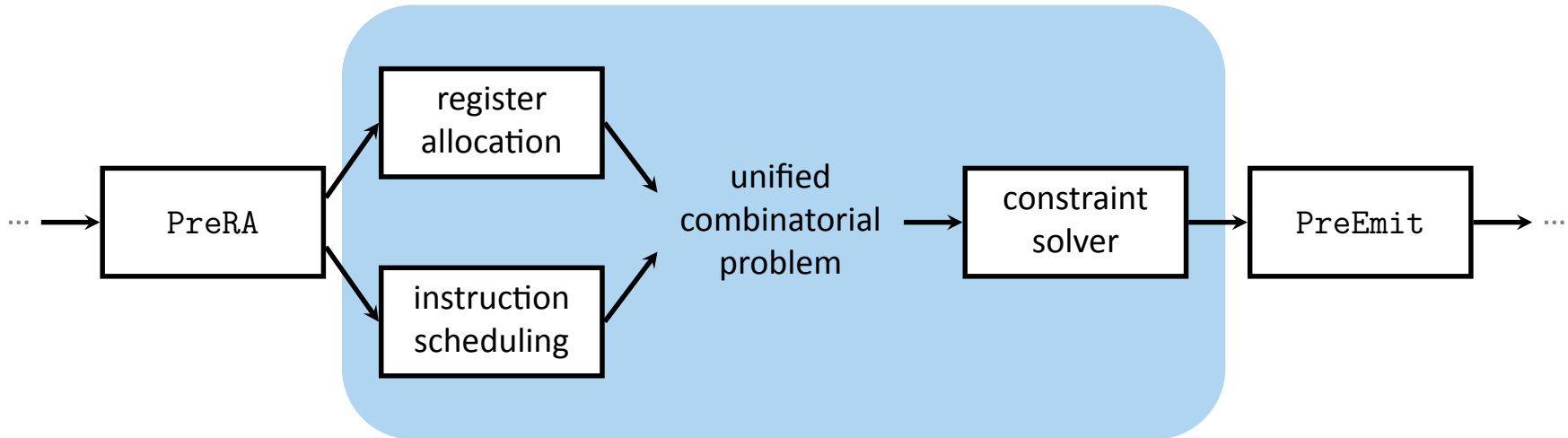

- Integration, combinatorial optimization

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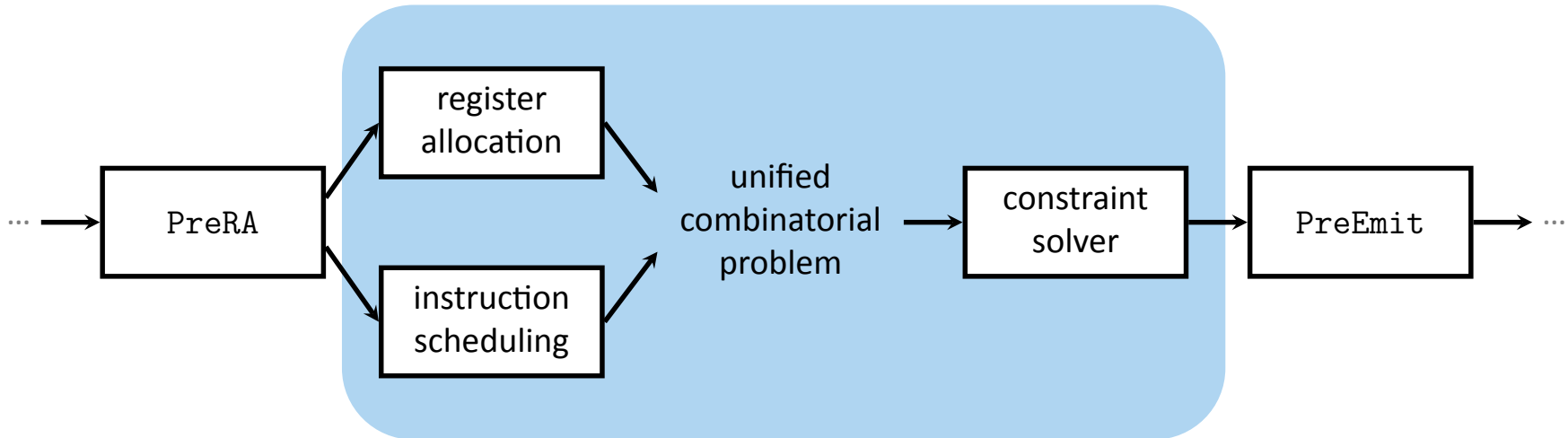

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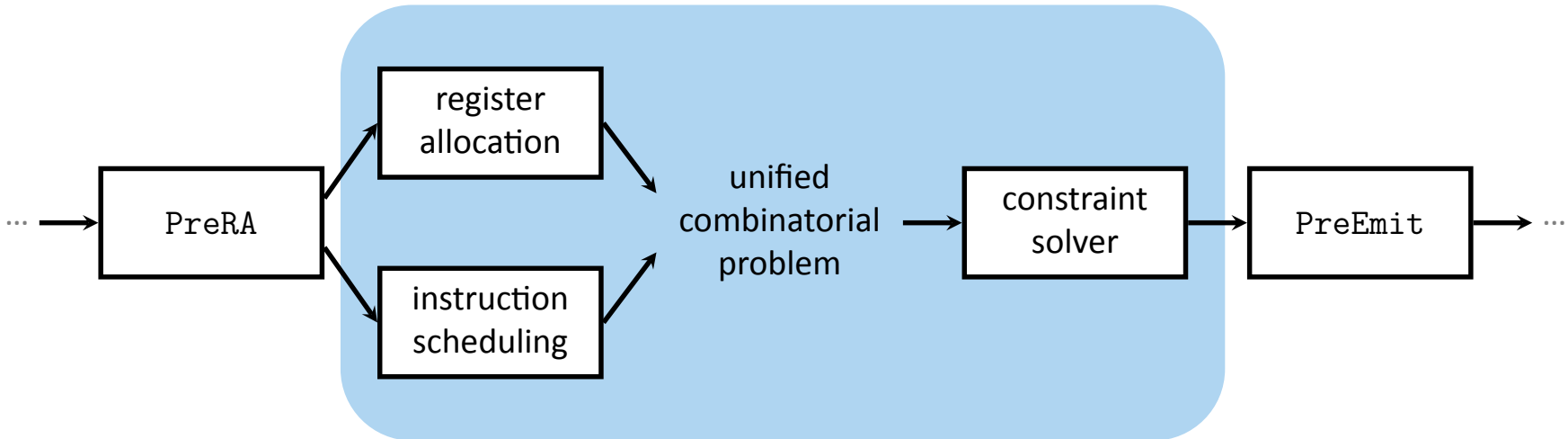

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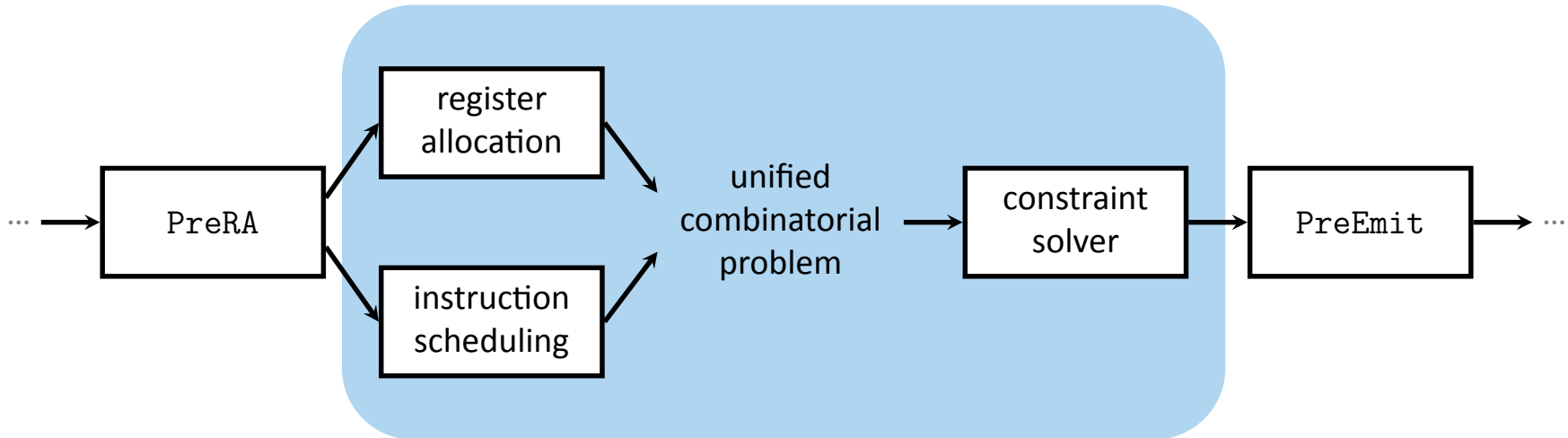

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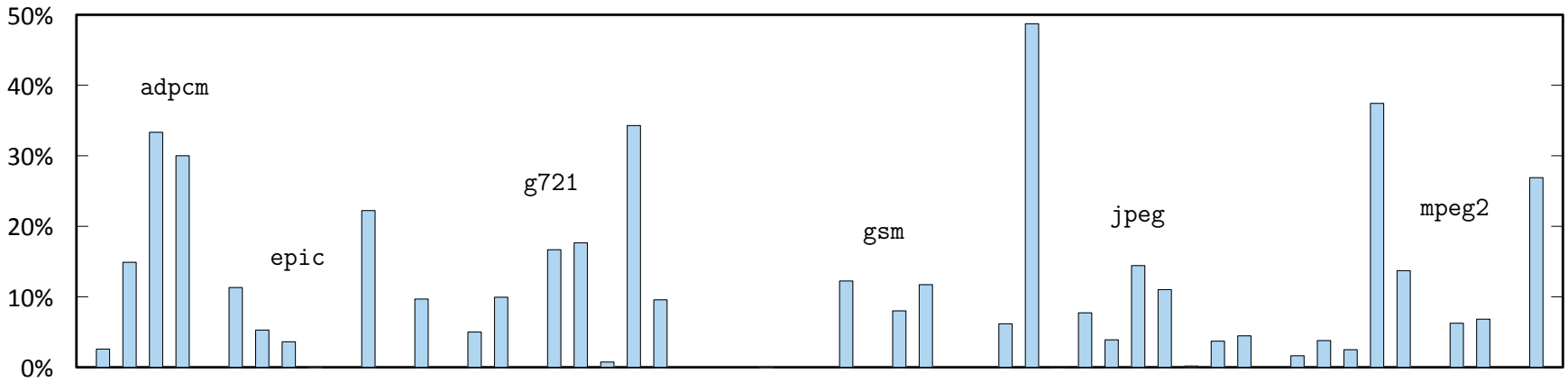
perfect complement to LLVM!

Speedup over LLVM 3.8



- 50 MediaBench functions
- Hexagon V4 processor

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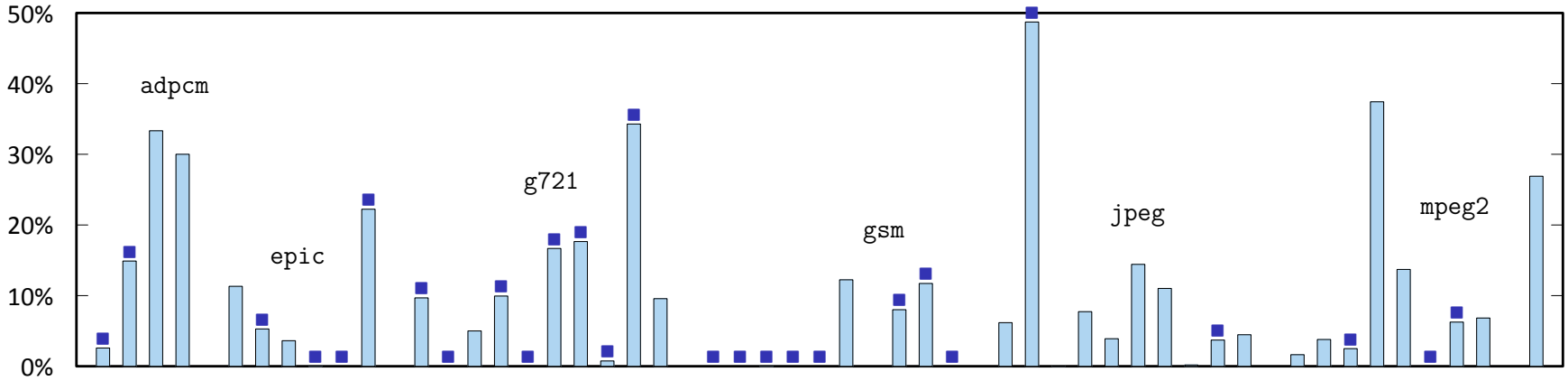

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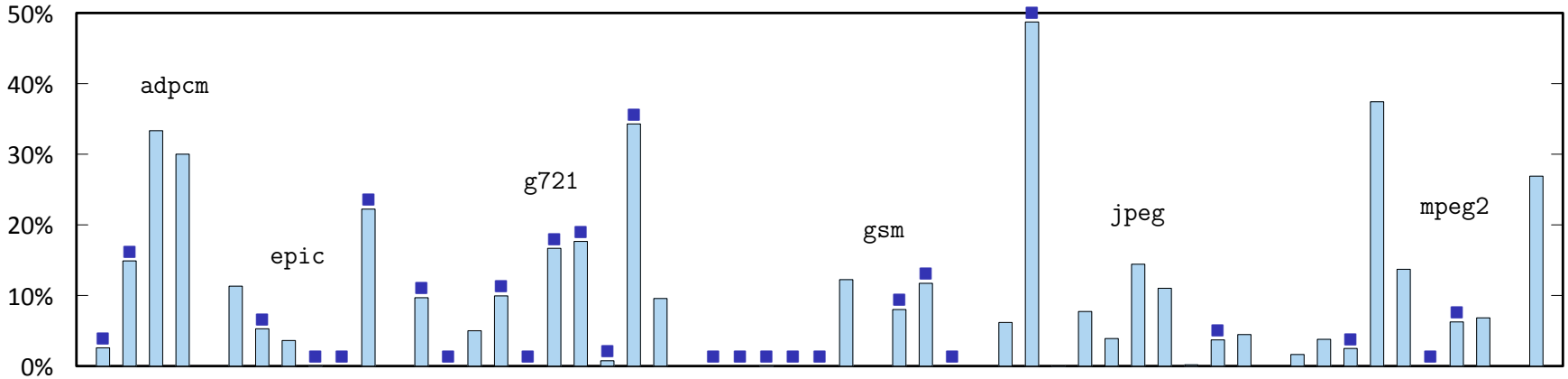

- 50 MediaBench functions
- Hexagon V4 processor
- Provably optimal (■) for 54% of the functions
- Compilation time: from seconds to minutes

Unison Is Practical and Effective

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  - register allocation
  - instruction scheduling

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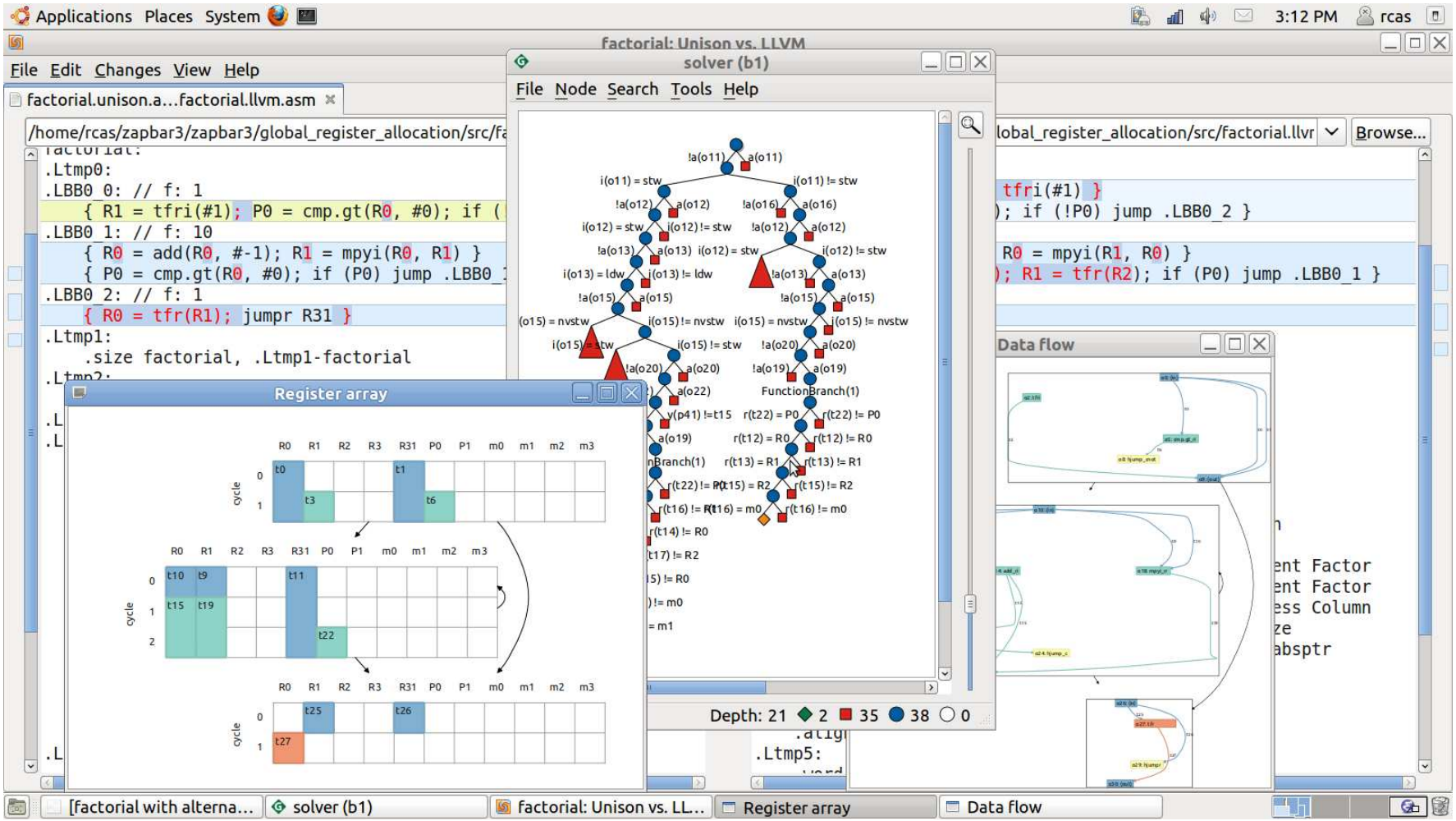
- Complements LLVM:
  - traditional LLVM for compile/debug cycle
  - LLVM + Unison for release builds
- Useful analysis tool for LLVM developers
  - how good is my heuristic?

Demo at CC2016 (12:20)



www.sics.se/~rcas/unison-demo