RISC-V: towards a reference LLVM backend

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What is RISC-V?

- A free to implement ISA originally developed at UC Berkeley
- Has Linux, QEMU, FreeBSD, seL4, Coreboot, ... ports
- 32-bit, 64-bit, 128-bit(!)
- Modular specification (scales up and down)
- See http://riscv.org

The opportunity

- Hardware/software co-design enabling rapid innovation from the open hardware community.
- Make LLVM more accessible to groups performing computer architecture research
- Improve documentation for the wider LLVM community

The approach

- Incremental, easily reviewable patches
- Start with the MC layer
- Maintain the patchset separately as a living artefact, even after merging
- Act as a ‘reference’ backend
- See github.com/lowRISC/riscv-llvm

Status

- Initial set of MC patches mostly reviewed and starting to be committed
- Follow-on patches for basic codegen will be posted in the next couple of weeks
- Docs/tutorial: currently exists in the form of copious notes. Needs to be cleaned up and shared

Future

- Complete codegen
- Benchmarking, optimisations
- LLDB, LLD, ...
- Support for RVC (compressed 16-bit instruction encoding)
- Prototype support for proposed vector extensions
- Tagged memory

Get involved

- Chat to me about how you can help (asb@lowrisc.org, or in person)
- Review patches
- Look at “RFC: Implement variable-sized register classes”