Look-Ahead SLP: Auto-vectorization in the presence of commutative operations

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Straight-Line Code Vectorizer

- LLVM and GCC provide SLP
  - Superword Level Parallelism [Larsen PLDI'00]
  - Bottom-Up SLP

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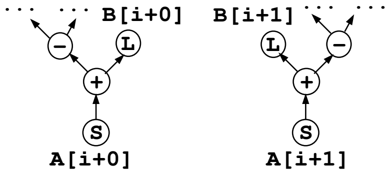
  - Even if loop vectorizer fails, SLP could partly succeed
- Compilers usually run SLP after the Loop Vectorizer

Why commutative operations matter ?

- Operands can be reordered
- It can change the shape of the DAG
- Since SLP operates on DAGs, it affects the SLP's vectorization effectiveness

```
sub1 = ... - ...;
sub2 = ... - ...;
A[i+0] = sub1   + B[i+0];
A[i+1] = B[i+1] + sub2;
```

DAGs



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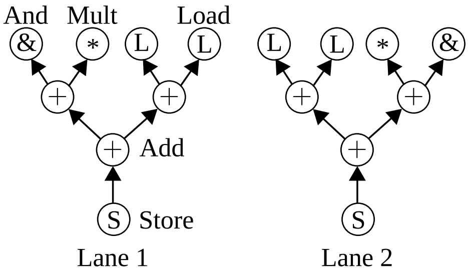
  3. Reodering across chains of commutative operations*
- Look-Ahead SLP (LSLP) provides a solution to all three.

Reordering Chains of Commutative Operations



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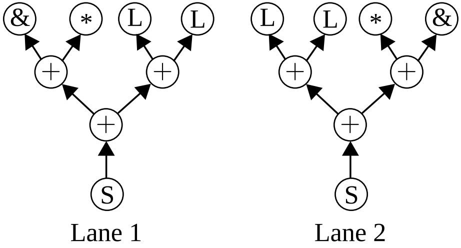

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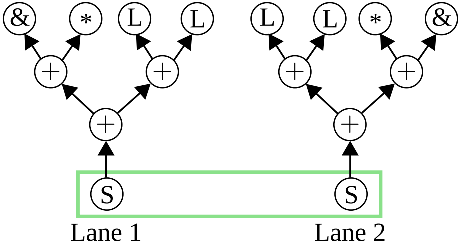

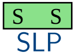

🟥 Non−Vectorizable 🟩 Vectorizable +/−#Cost

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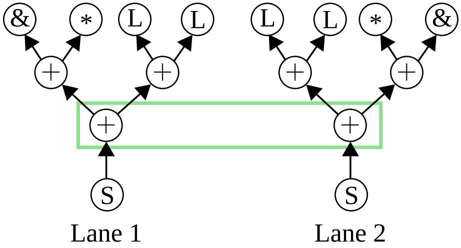

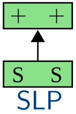

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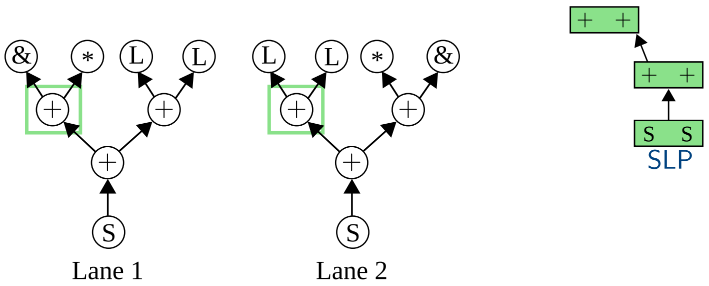

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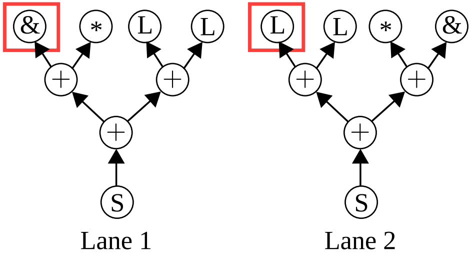

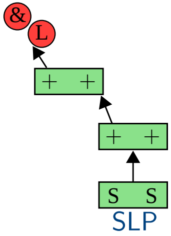

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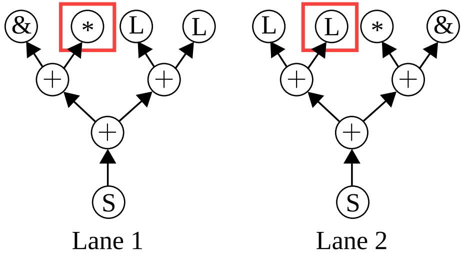

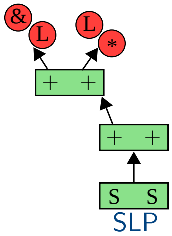

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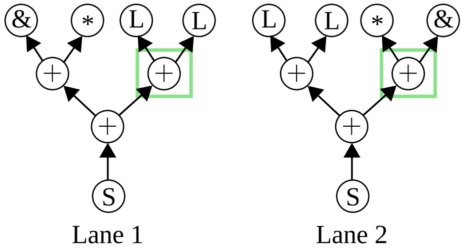

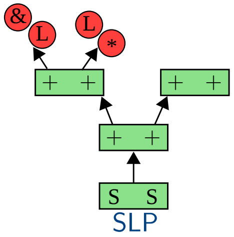

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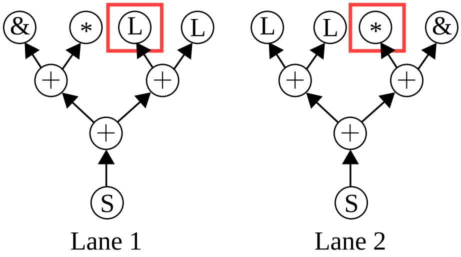

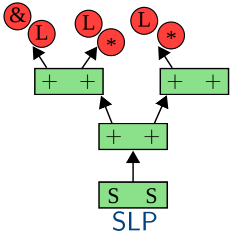

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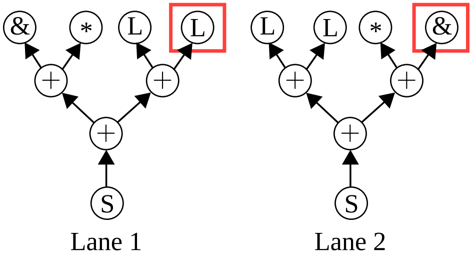

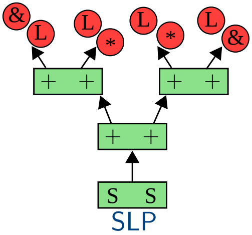

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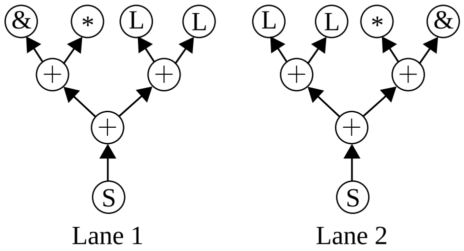

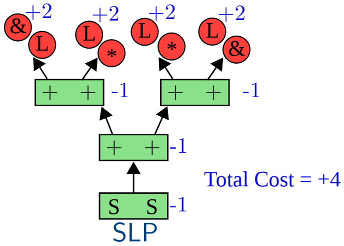

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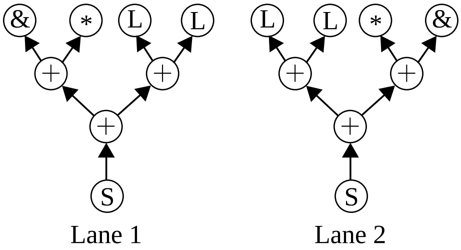

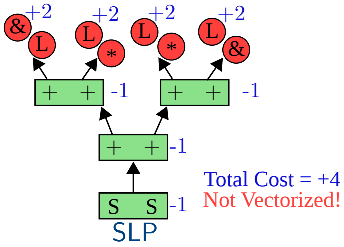

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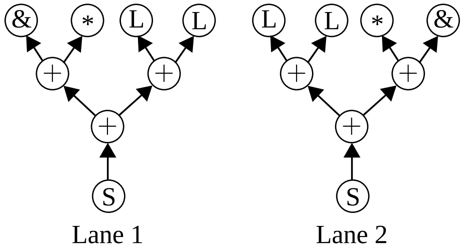

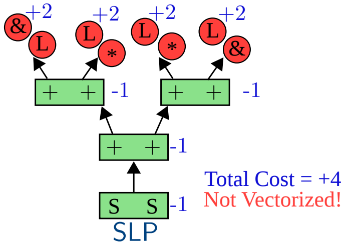

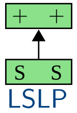

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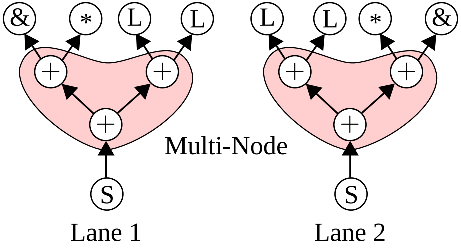
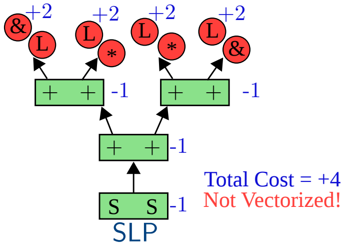
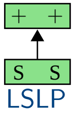




Total Cost = +4
Not Vectorized!



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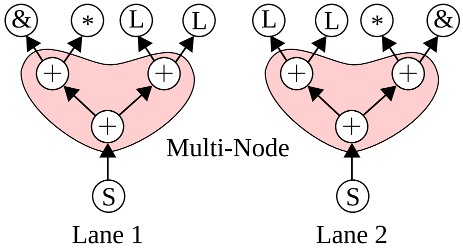

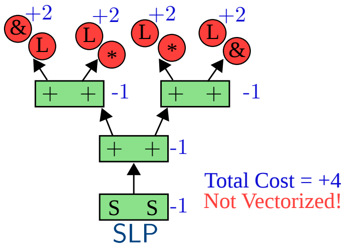

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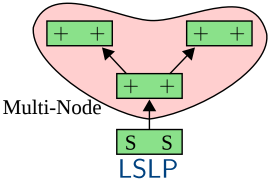

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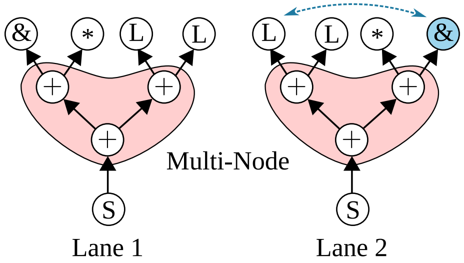

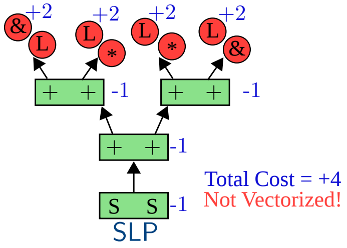

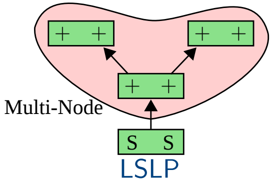

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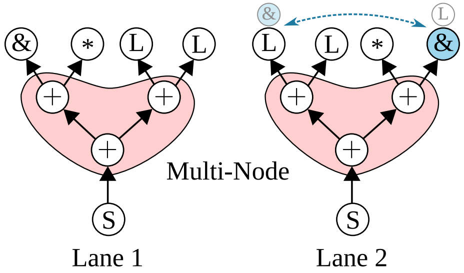

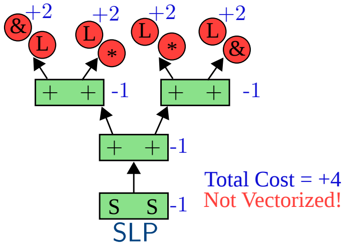

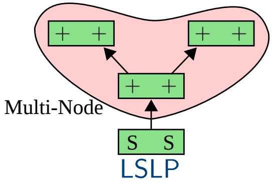

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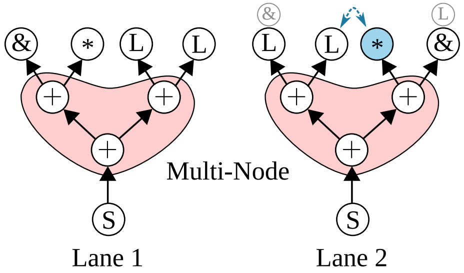

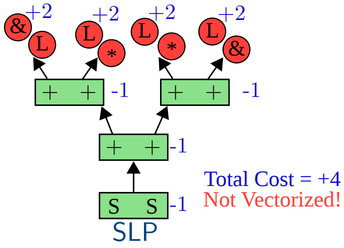

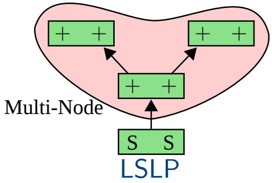

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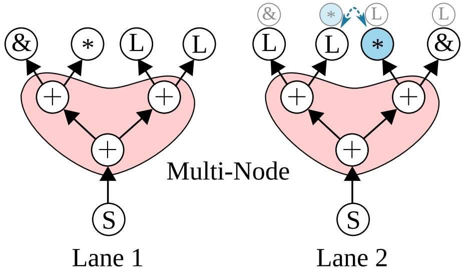

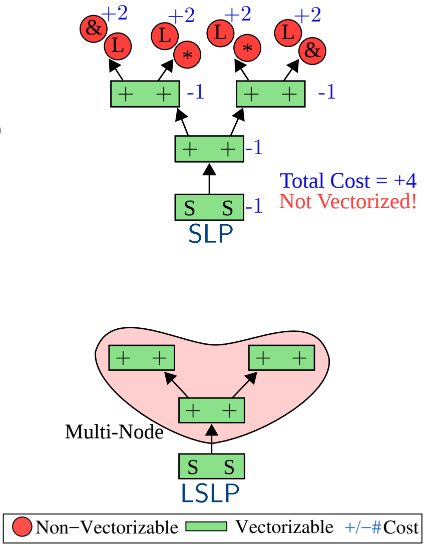

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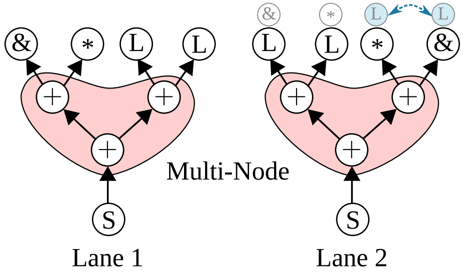

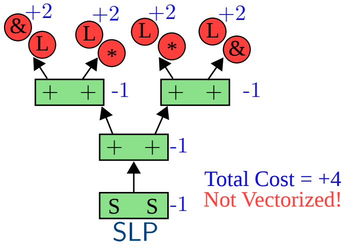

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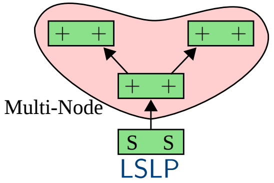

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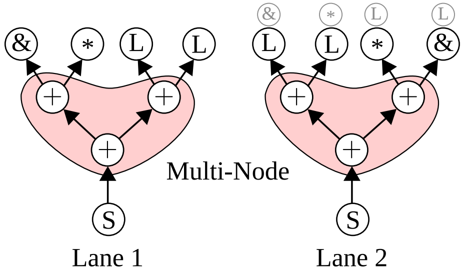

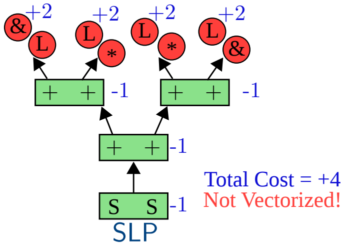

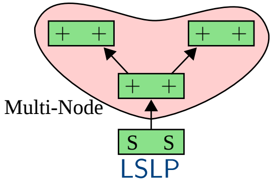

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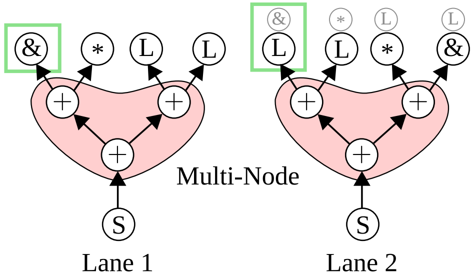

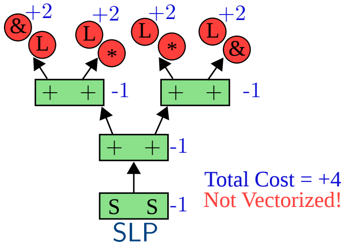

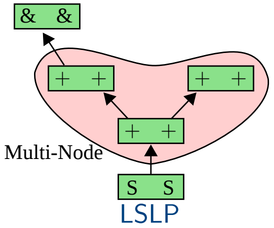

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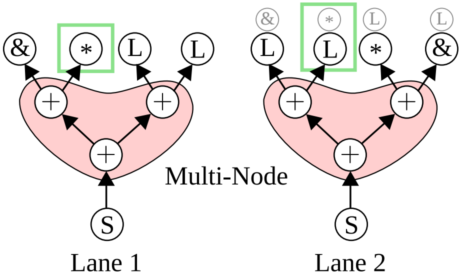

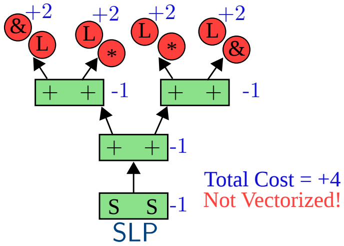

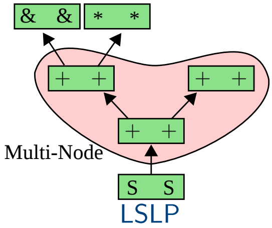

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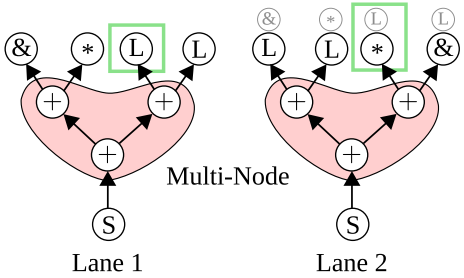

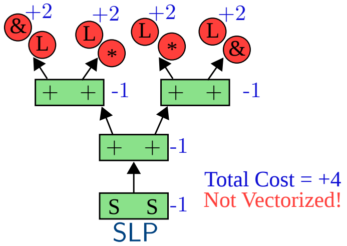

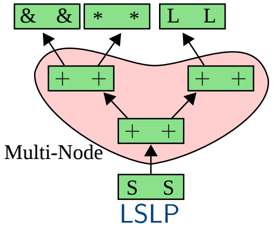

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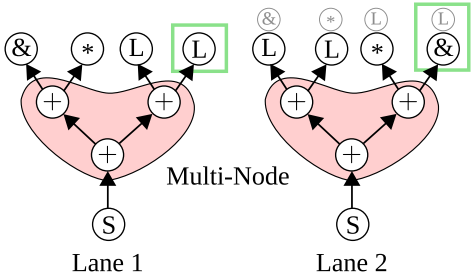

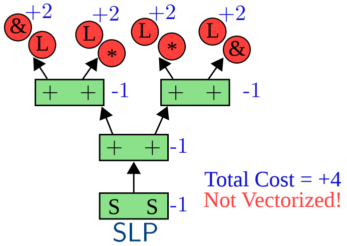

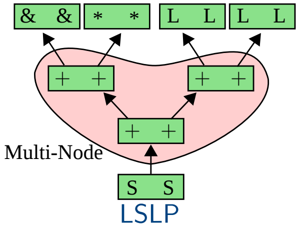

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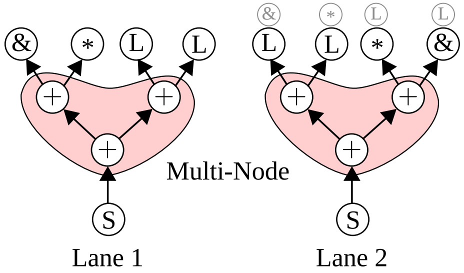

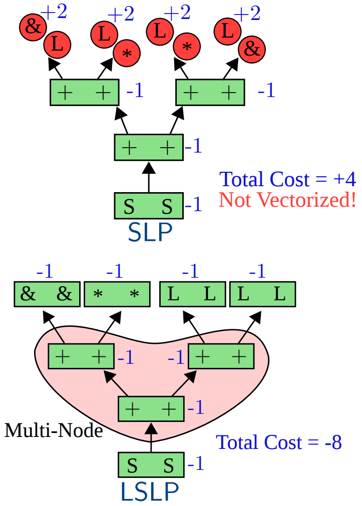

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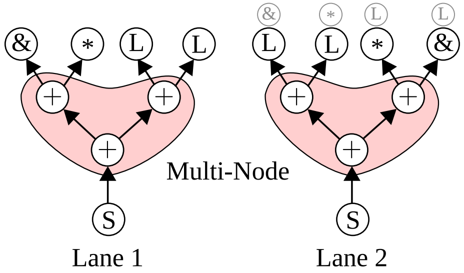

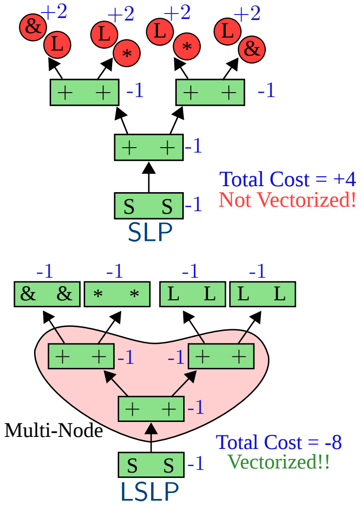

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Experimental Setup

- Target: Intel Core i5-6440HQ Skylake CPU
- Kernels from SPEC CPU2006
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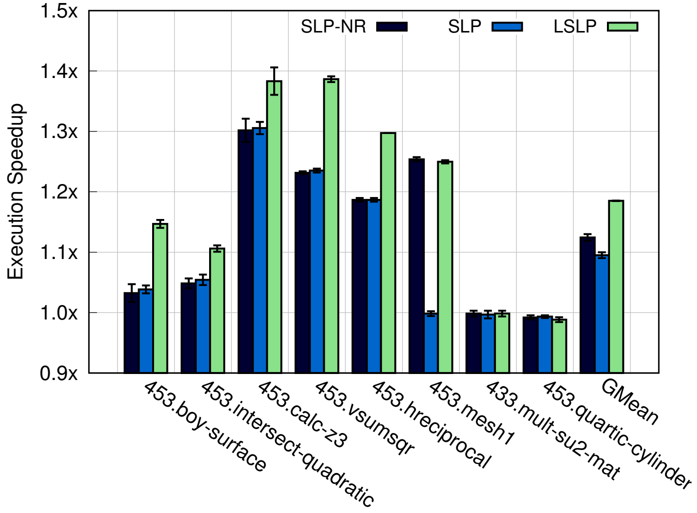
Performance (normalized to O3)



Conclusion

- LSLP introduces an effective scheme for dealing with commutative operations.
- Look-Ahead SLP: Auto-vectorization in the presence of commutative operations (CGO 2018)