MIR Support in LLVM-reduce

Matt Arsenault
Motivation

• Deluge of assertions and verifier errors in register allocation
• Very sensitive to any minor code changes
• IR reduction alone is inadequate
  • Often cannot get below thousands of IR instructions
• These kinds of failures bit rot incredibly quickly
  • Important to get a minimal MIR reproducer quickly
• Fractal explosion of other failures found during reduction process
Usage

$ llvm-reduce -mtriple=amdgcn-amd-amdhsa -mcpu=gfx900 --test=./run_llc.sh failure.mir

#!/bin/bash
! llc -mtriple=amdgcn-amd-amdhsa -mcpu=gfx900 -start-before=simple-register-coalescing -stop-after=greedy,1 -verify-machineinstrs $@

#!/bin/bash
llc -mtriple=amdgcn-amd-amdhsa -mcpu=gfx900 -start-before=machine-scheduler -stop-after=greedy,1 -verify-regalloc $@ 2>&1 | grep -m1 "Cannot decrease cascade number, illegal eviction"
Reduction Implementation

```c++
static void extractInstrFromModule(Oracle &O, ReducerWorkItem &WorkItem) {
    for (const Function &F : WorkItem.getModule()) {
        if (MachineFunction *MF = WorkItem.MMI->getMachineFunction(F))
            extractInstrFromFunction(O, *MF);
    }
}
```
MIR vs. IR

• More difficult to produce plausibly valid MIR

• Really 3 IRs in one
  • Generic MIR
  • Selected SSA
  • Post-SSA
MIR vs. IR

• Virtual registers are not a direct replacement for Values
  • Cannot simply replace deleted values with undef/poison
  • Need to find a valid place to place IMPLICIT_DEF
• Need to consider register liveness
• Different control flow graph (CFG) representation
  • IR BasicBlocks implicitly track CFG through block references in terminator instructions
  • MachineBasicBlocks directly track successors and predecessors
  • Fall-through blocks
  • Terminators may not be analyzable
  • No undef blocks
    • Use dummy empty block inserted at the end of the function
• Additional properties not represented in the IR
Reduction Passes

Instructions
Reduce Uses / Defs
Instructions can have multiple results
Insert replacement IMPLICIT_DEFs
Delete implicit operands post SSA
Reduce IR References - Eliminate IR references
MachineMemOperands
FrameIndexes derived from alloca
IR BasicBlock names
Register hints
Register masks
Instruction flags
Target Support

- MachineFunctionInfo::clone
  - Most implementations trivial
- Register and frame index values remain unchanged
- Needs to remap any pointer values
  - MachineBasicBlocks

```cpp
MachineFunctionInfo *
SIMachineFunctionInfo::clone(
    BumpPtrAllocator &Allocator,
    MachineFunction &DestMF,
    const DenseMap<MachineBasicBlock *, MachineBasicBlock *> &Src2DstMBB) const {
    return DestMF.cloneInfo<SIMachineFunctionInfo>(*this);
}
```
Machine Verifier Issues

- Verifier optionally checks LiveIntervals
  - Uses separate, buggier liveness checks without it
  - Fails to catch missing defs in the entry block
  - Fails to catch subregister issues
    - [https://reviews.llvm.org/D127104](https://reviews.llvm.org/D127104) - MachineVerifier: Add test which the verifier incorrectly accepted before
  - Different failures with and without LiveIntervals
  - Ambiguously valid MIR - cases which only trigger a verifier error if subregister liveness is enabled
- Chicken and egg failures with LiveIntervals
  - LiveIntervals construction not expecting to handle invalid IR
  - Doesn’t handle unreachable blocks
Remaining Infrastructure Issues

• Targets not fully serializing MachineFunctionInfo
• Some generic fields still not serialized
• LiveIntervals calculation modifies the MIR
  • Sometimes splits new virtual registers
  • Introduces new dead flags
• MachineModuleInfo still has some stateful clutter, but mostly harmless
• -start-before/-stop-after work poorly with failures involving multiple functions
Experiences

• Block reduction pass not yet upstream
  • Highest value reduction
• Managed to make forward progress with difficulty
  • Still much better than manual reduction
  • Manual adjustments to blocks
• Had to run individual reductions to avoid some of the failures
  • Deleting def reduction too slow without liveness consideration
• Behaves like a MIR fuzzer
  • Unsurprisingly, many bugs with undef register handling
Future Needs

- Get work item verification to use LiveIntervals
- Rewrite block reduction to use LiveIntervals to find live registers and get upstream
- CFG simplification pass - not the same as block reduction
  - Fallthrough blocks and trivial successors may matter
- No attempt to handle reducing physical register uses/defs
Outstanding Reviews

• [https://reviews.llvm.org/D127107](https://reviews.llvm.org/D127107) llvm-reduce: Add reduction pass for MachineBasicBlocks

• [https://reviews.llvm.org/D127108](https://reviews.llvm.org/D127108) llvm-reduce: Handle reducing blocks using G_BR/G_BRCOND

• [https://reviews.llvm.org/D127103](https://reviews.llvm.org/D127103) CodeGen: Split out MachineVerifier's liveness tracking
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