An approach to sustainably add Vector Predication to the Loop Vectorizer

Lorenzo Albano <lorenzo.albano@bsc.es>
Roger Ferrer <roger.ferrer@bsc.es>

Background
The Loop Vectorizer does not make use of Vector Predication intrinsics. We have been extending the Loop Vectorizer with new Vector Planner recipes that are vector length and mask aware. This approach works but leads to recipes duplication in the Loop Vectorizer.

We wanted to see if a simpler approach is workable.

Method
We implemented a new mode of tail folding in the Loop Vectorizer to only emit the minimum Vector Predication intrinsics needed for correctness: memory accesses and a (target-dependent) set vector length mechanism that depends on the remaining iterations of the loop.

A later pass analyses what is demanded from the vectors, starting from Vector Predication stores. From this analysis, vectorized IR instructions (when possible) are replaced with Vector Predication intrinsics that use the demanded vector length and mask.

Results
We have used the TSVC-2 benchmark and the RISC-V target. We have compared the emitted code against our earlier, more invasive, implementation. The emitted code is comparable to our previous implementation.

Conclusion
This approach requires a small set of changes to the Loop Vectorizer while allowing us to reason about vector length and predicate in another pass.

This approach is low cost and benefits RISC-V and VE targets, that have vector length, and SVE and AVX-512 targets that can now make a more effective use of their predicated ISAs.

Using Vector Predication does not mean we have to duplicate all the concepts in the Loop Vectorizer.