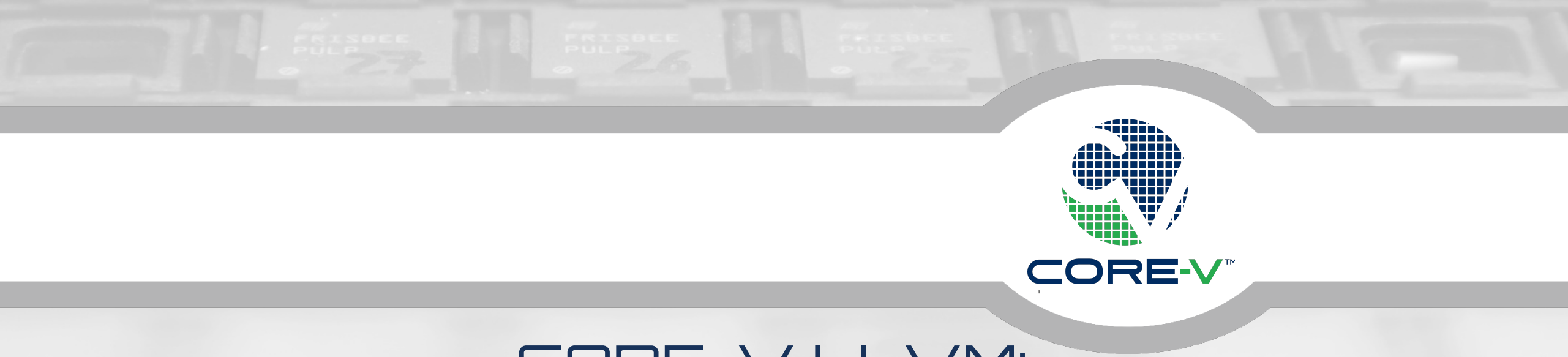

CORE-V LLVM: Adding eight vendor extensions to standard RISC-V LLVM

Charlie Keaney, Chunyu Liao, Lewis Revill

About OpenHW Group

CORE-V®

Collaborators

CORE-V™

EMBECOSM®

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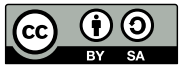
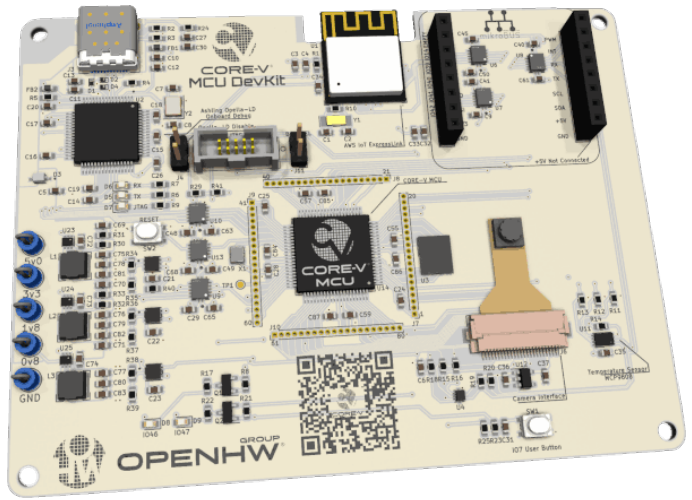
Institute of Software Chinese Academy of Sciences

OPENHW GROUP™
PROVEN PROCESSOR IP



About CV32E40P



- Post-incrementing load/store (25)
- Hardware loops (6)
- General ALU operations (31)
- Immediate branching operations (2)
- Multiply-accumulate (22)
- PULP SIMD (220)
- PULP Bit manipulation (16)
- Event Load (1)

Goal

Approach

Linker

Libraries

Code generation

Assembler

Challenges

- No Builtin Spec
- GNU Compatibility
- Testing
- No Silicon
- Training a new generation

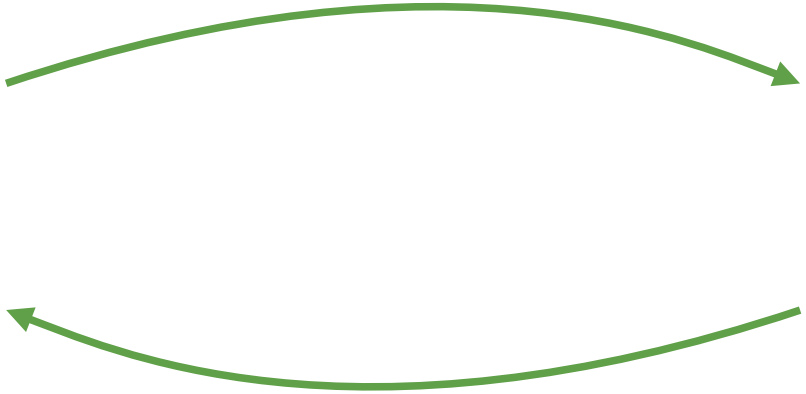
Do all instructions need builtins?

No Builtin spec

What do we name the builtins?

What builtins do we include?

GNU Compatibility



Testing

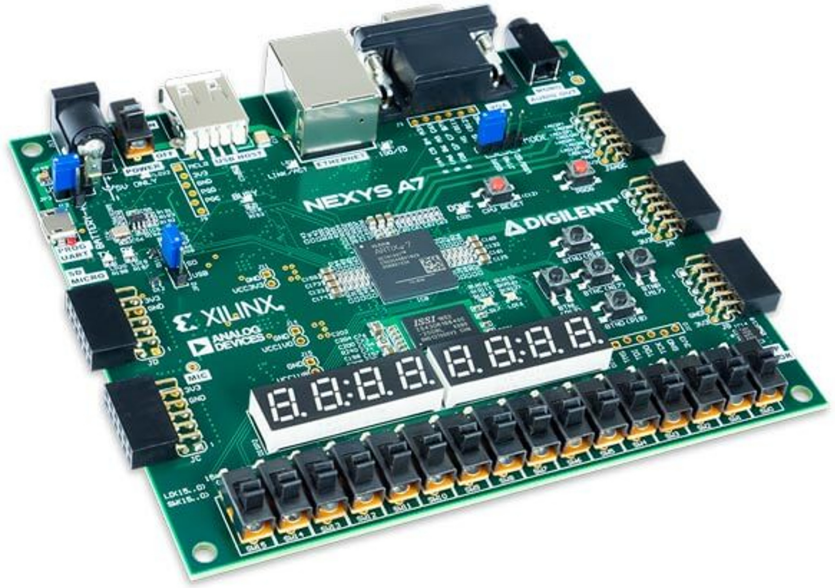
LLVM LIT

GCC Regression

Gas comparison

Continuous Integration

Pre-silicon Testing



VERILATOR

Training a new generation

Join us!

- As a user
  - embecosm.com/resources/tool-chain-downloads
  - Pre-built binaries, source code, scripts and test results
- As a developer
  - Join the OpenHW Mattermost SW : LLVM Tools channel
  - Sign up to the OpenHW SW mailing list and attend the monthly meeting
  - Attend the weekly CORE-V LLVM Tools Engineering call
- CORE-V source code
  - github.com/openhwgroup/corev-llvm-project