Developing An LLVM Backend For VLIW RISC-V Vector Extension Architectures

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VLIW RISC-V Vector Extension Architecture

ResMII with LMUL Factor for Swing Modulo Scheduling

Assume each instruction latency is 1, the ResMII will be set to 1. However, the LMUL will group multiple registers and affect operation latency in some processor implementation. The resource conflict might happened at cycle 3 when the latency of vector operation is larger than 1. As a result, the ResMII should be modified.

Experimental Results

Benchmark : DSPstone
LLVM version : LLVM 15
Simulator : Spike

In this code generation flow, we add DFAPacketizer to group instructions into an instruction bundle and rewrite RISCVAsmPrinter to emit instruction bundle with the custom instruction we use to imply the beginning of the bundle.

b. Codegen example

```
for(int i = 0 ; i < X ; i++)
{
    s = A[i];
    A[i] = s * 42 + 3;
}
```

```
package zero, 0
# hhn.18
package zero, 0

for(int i = 0 ; i < X ; i++)
{
    s = A[i];
    A[i] = s * 42 + 3;
}
```